



You don't have to be an engineer to be a racing driver, but you do have to have **mechanical sympathy**

Sir Jackie Stewart - three-time F1 world champion

Mechanical Sympathy Applied to IT

- Concept applied to software by Martin Thompson
- As developers, we **don't need** to be hardware engineers
- Yet, having an understanding of how does a machine work can make us a **better developer** (algorithms, data structures)

Today: How to be a better Go developer by understanding how CPUs are working









Teiva Harsanyi **y**teivah

Software Engineer - Beat

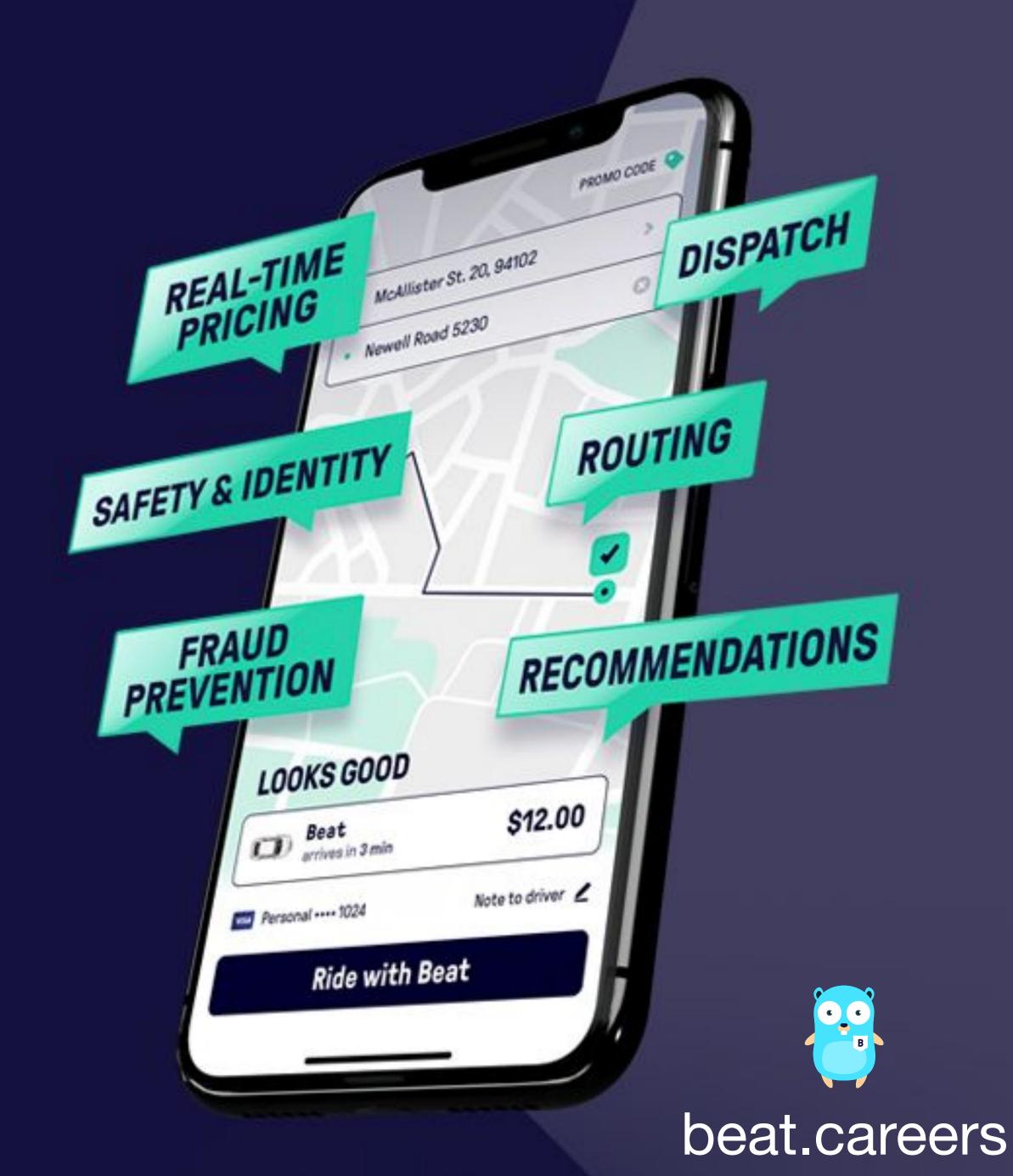


HIRING SOFWARE

ON CUTTING-EDGE TECHNOLOGIES

DISCOVER YOUR NEXT CHALLENGE IN AMSTERDAM, ATHENS OR REMOTE



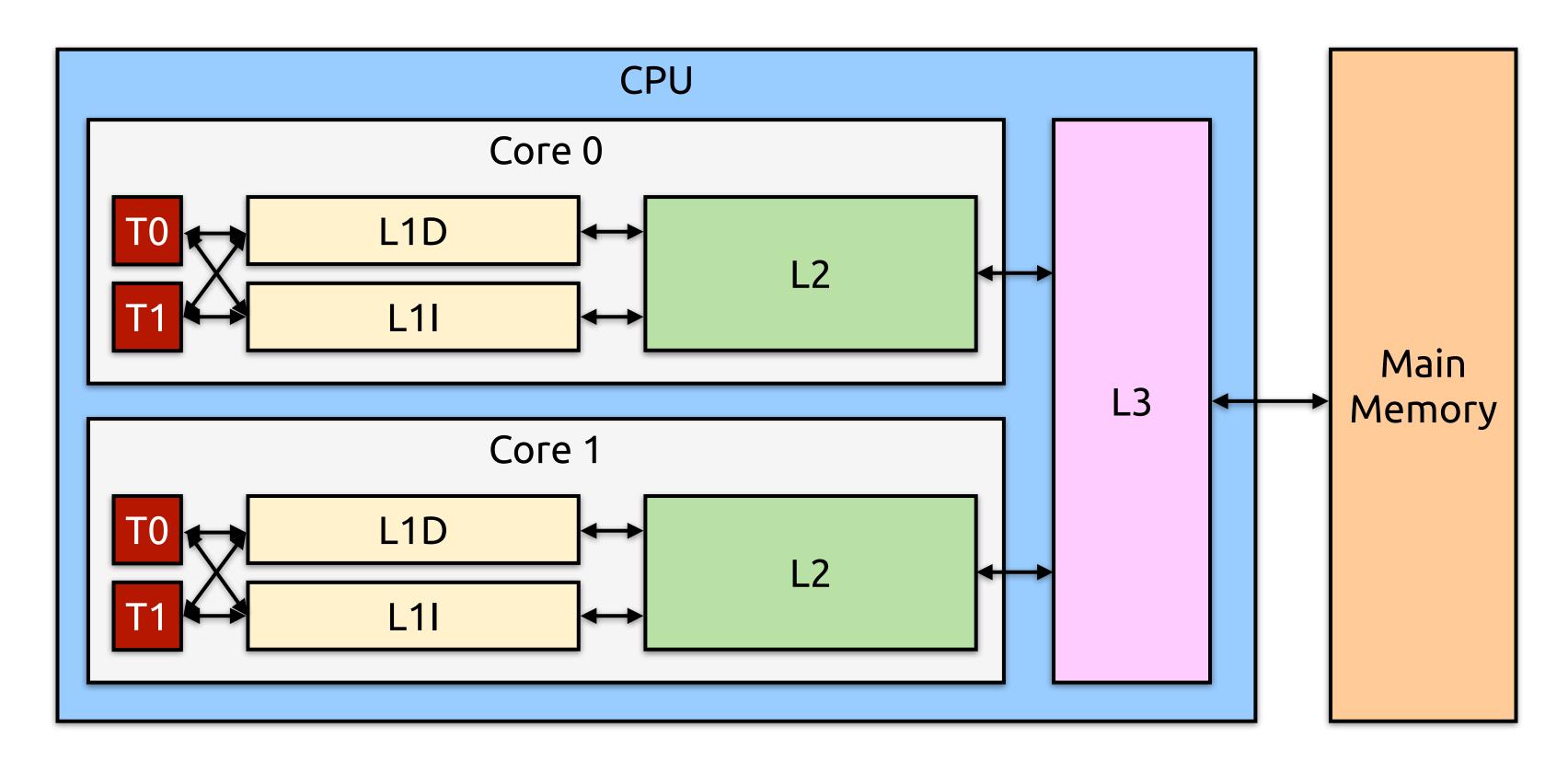




CPU Architecture Locality of Reference **Data-Oriented Design** Caching Pitfall Concurrency



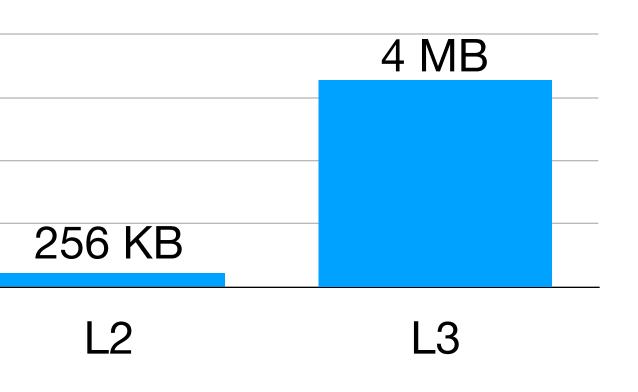
CPU Architecture - Intel Core i5-7300



Cache size

32 KB

L1D/L1I



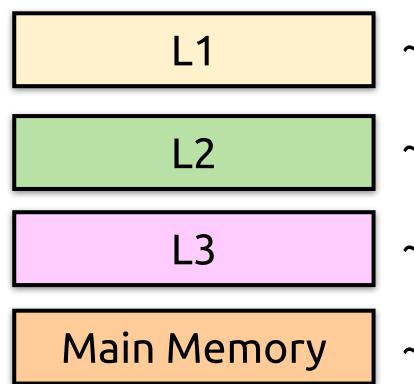


CPU Architecture - Intel Core i5-7300

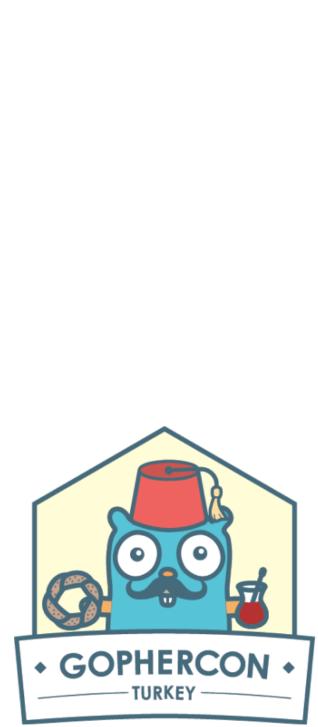




As a developer, I would like my application to leverage CPU caches



- ~1 ns
- ~3 times slower than L1
- ~10 times slower than L1
- ~50/100 times slower than L1



CPU Architecture Locality of Reference **Data-Oriented Design** Caching Pitfall Concurrency



Locality of Reference

If a **particular memory location** is referenced, it is **likely** that...

Temporal Locality

> Spatial Locality



The same location will be referenced again in a near future

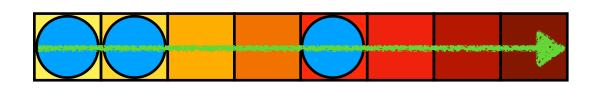
Nearby memory locations will be referenced in a near future

sum := 0 s := initSliceOfInts() length := len(s)SUM += S[i]

for i := 0; i < length; i++ {</pre>



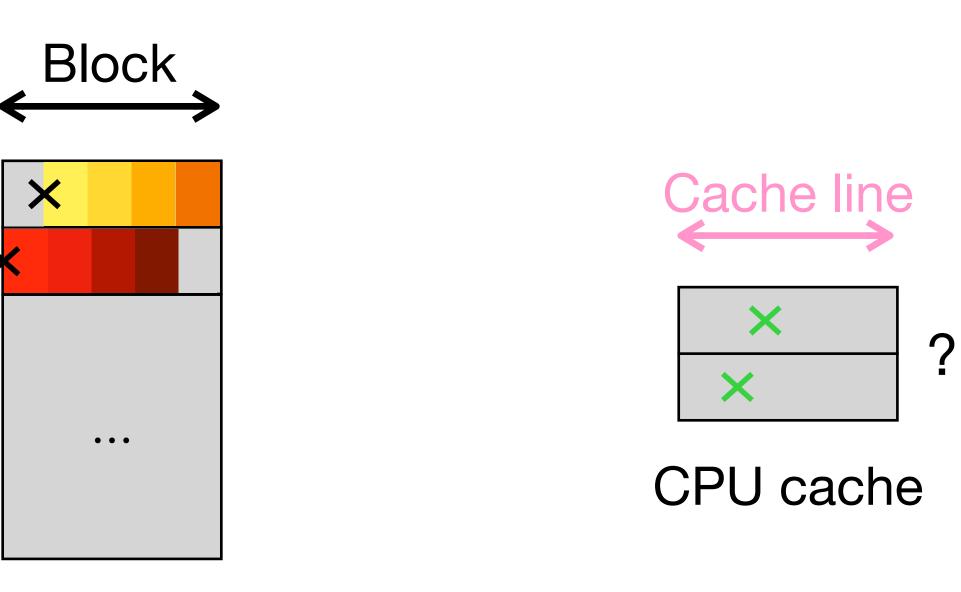
Spatial Locality



Slice (in our heads)

Matrix (main memory)

- Instead of copying a single variable, the processor will copy a cache line
- Cache line: contiguous segment of memory of a fixed size (usually 64 bytes)
- Limited number of cache miss (compulsory miss)
- Theory (other applications can run at the same time on the same core)
- Cache placement policy (L1, L2 or L3?)





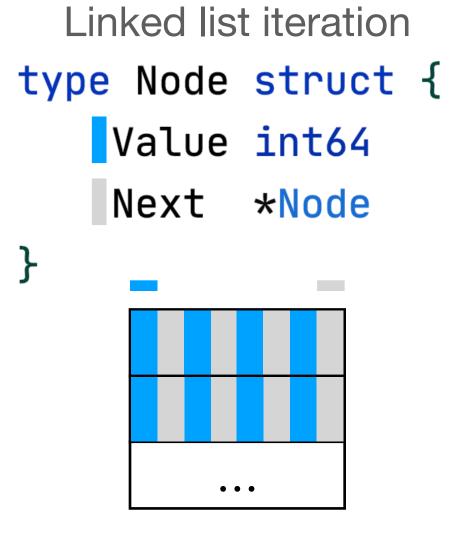
Helping the CPU

• To help the CPU, an application needs to leverage locality of reference

• ... and predictability



Linked List Iteration



Main memory

~230% slower



- **Possible** spatial locality
- But **not predictable** for the CPU (no line fetching)

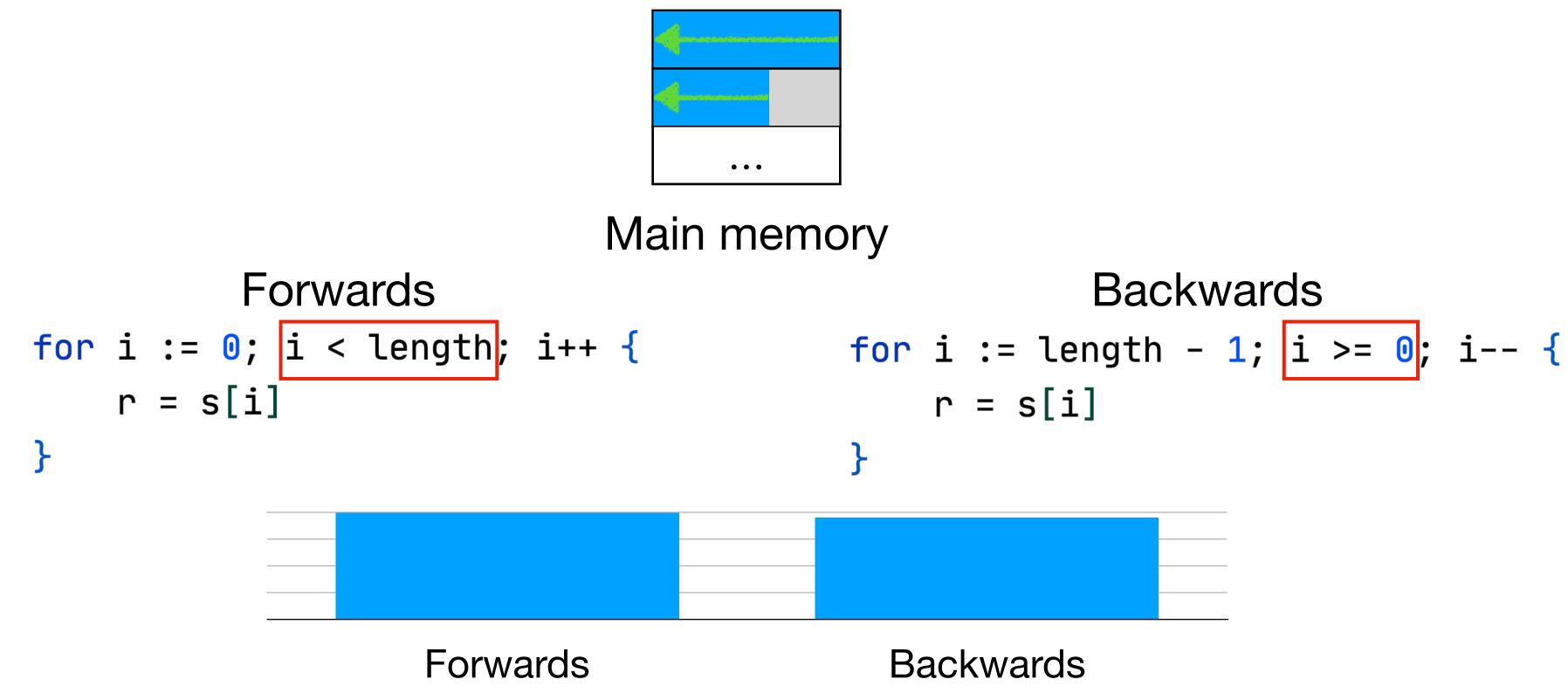
Iterating on a linked list that should be allocated contiguously should be decent

```
Slice iteration: one element out of two
 for i := 0; i < len(s); i+=2 {</pre>
     sum += s[i]
 }
                  • • •
         Main memory
   Slice iteration
```



Backwards Iteration

• What if we iterate **backwards** on a slice?



- Spatial locality \bullet
- The CPU was able to **predict** that we iterate backwards
- Slightly faster because the bound check is faster

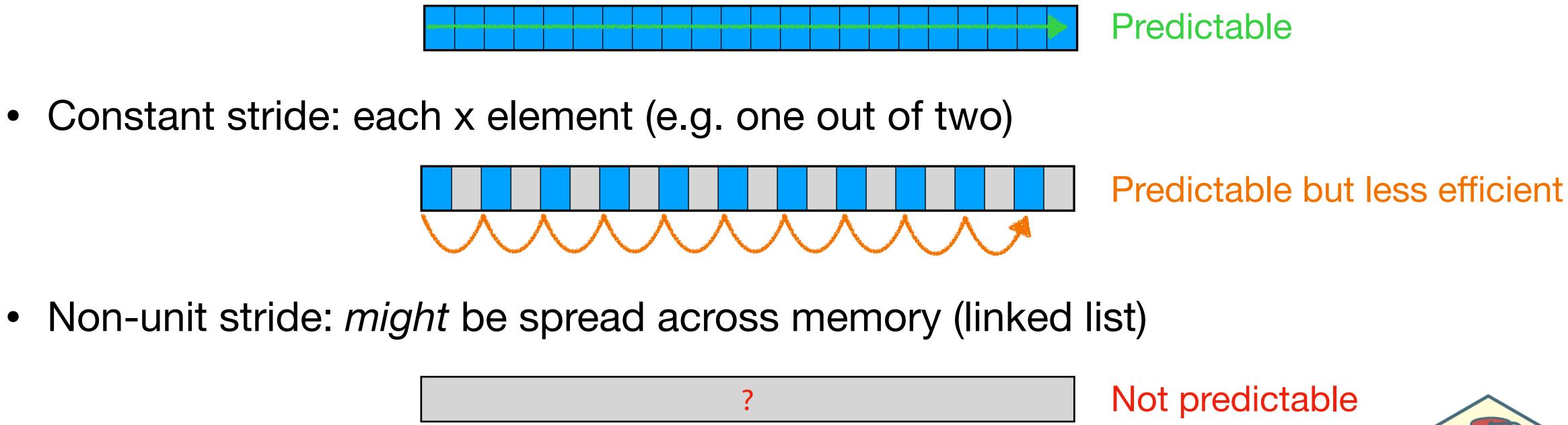




How to Make Things Predictable?

- Striding: how does a CPU work through our data?
 - Unit stride: each element

• Constant stride: each x element (e.g. one out of two)











- CPU caches are extremely fast
- A CPU doesn't cache a single variable but a cache line
- I can help the CPU if my application leverages: ullet
 - Locality of reference
 - Predictability



CPU Architecture Locality of Reference **Data-Oriented Design** Caching Pitfall Concurrency



Data-Oriented Design

from one form to another" - Mike Acton

- Yet, hardware does not like objects

of each cache line

"The purpose of all programs and all parts of those programs is to transform data

Object-Oriented design is a way to mirror how we interact with the real world

Data-Oriented design is about organising data in a way to get the most value out





Data-Oriented Design

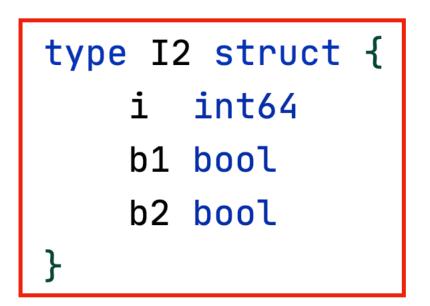
- 2 concrete examples:
 - Structure alignment
 - Slice of structures vs structure of slices



Structure Alignment

type I1 struct {
 b1 bool
 i int64
 b2 bool
}

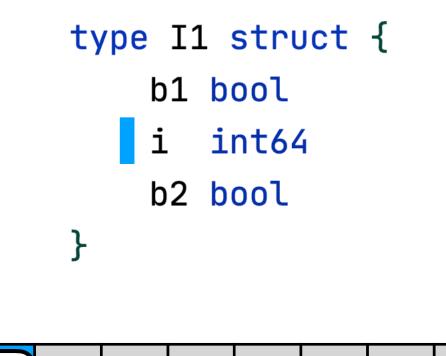
func BenchmarkI1(b *testing.B) {
 s := make([]I1, it)
 var r int64
 b.ResetTimer()
 for j := 0; j < it; j++ {
 r += s[j].i
 }
 result = r
}</pre>

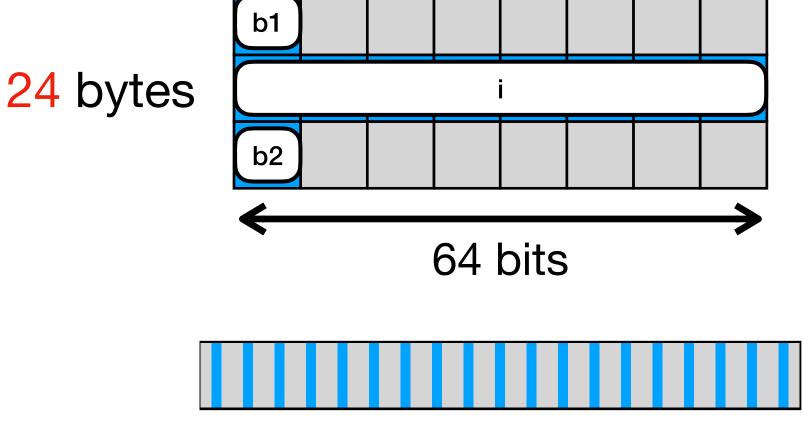


```
func BenchmarkI2(b *testing.B) {
    s := make([]I2, it)
    var r int64
    b.ResetTimer()
    for j := 0; j < it; j++ {
        r += s[j].i
    }
    result = r
}</pre>
```



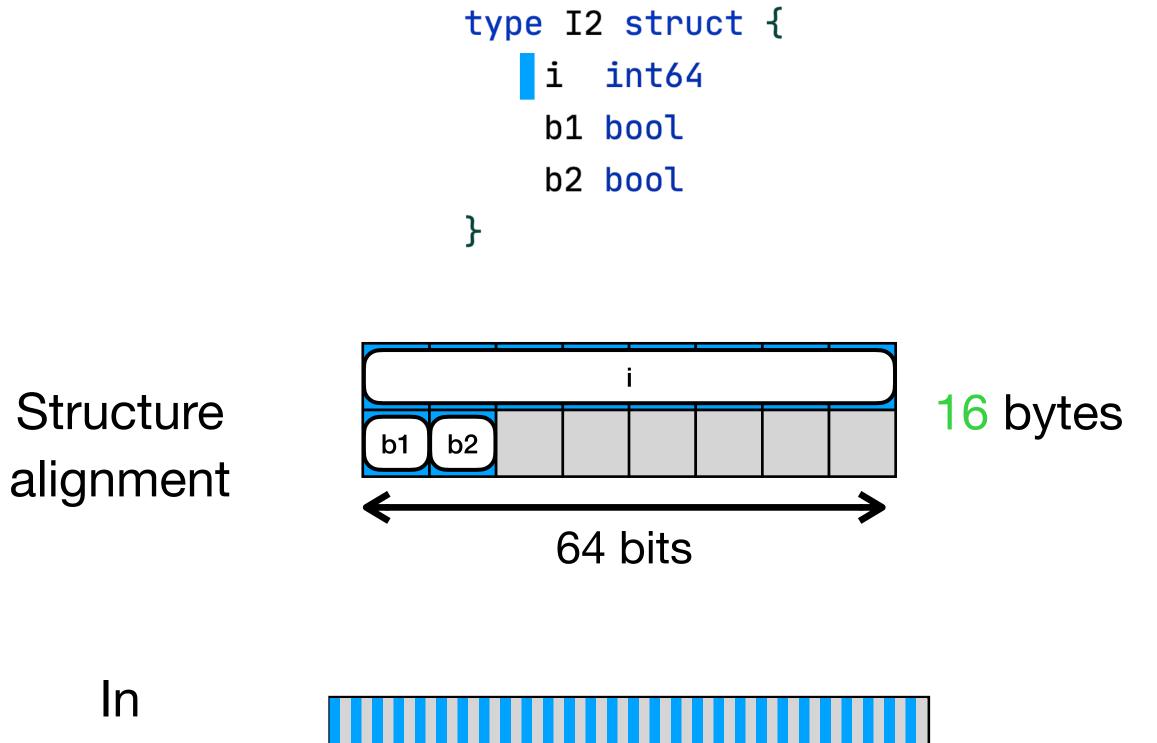
Structure Alignment





10k slice: 3750 cache lines (cache line: 64 bytes)

• The size of a structure is a multiple of the word size (64 bits on a 64-bit, etc.)

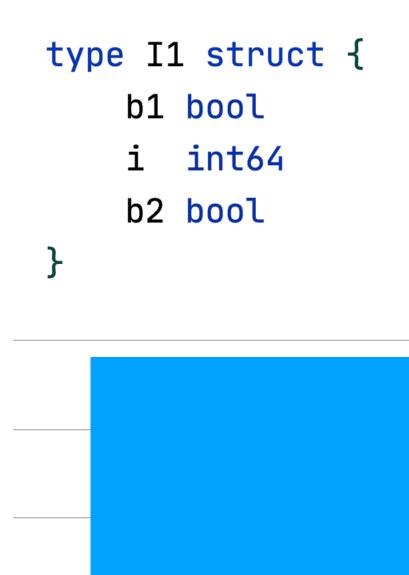


memory

10k slice: 2500 cache lines



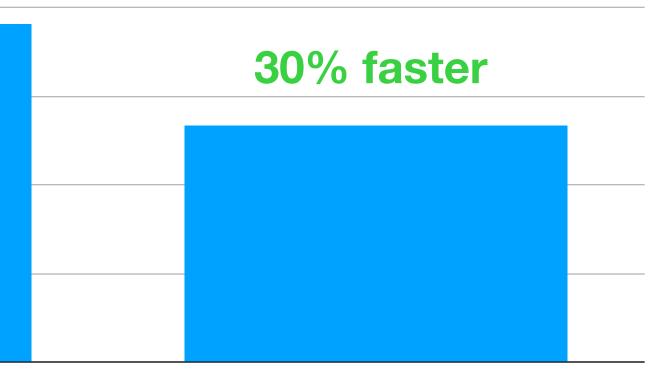
Structure Alignment



Not compact

- Memory footprint (GC pressure)
- Iterating over a **compact** data structure is more efficient as it requires less caches lines

```
type I2 struct {
    i int64
    b1 bool
    b2 bool
}
```



Compact



type Struct1 struct {
 a int32

b int64

}

func BenchmarkSliceOfStructures(b *testing.B) {

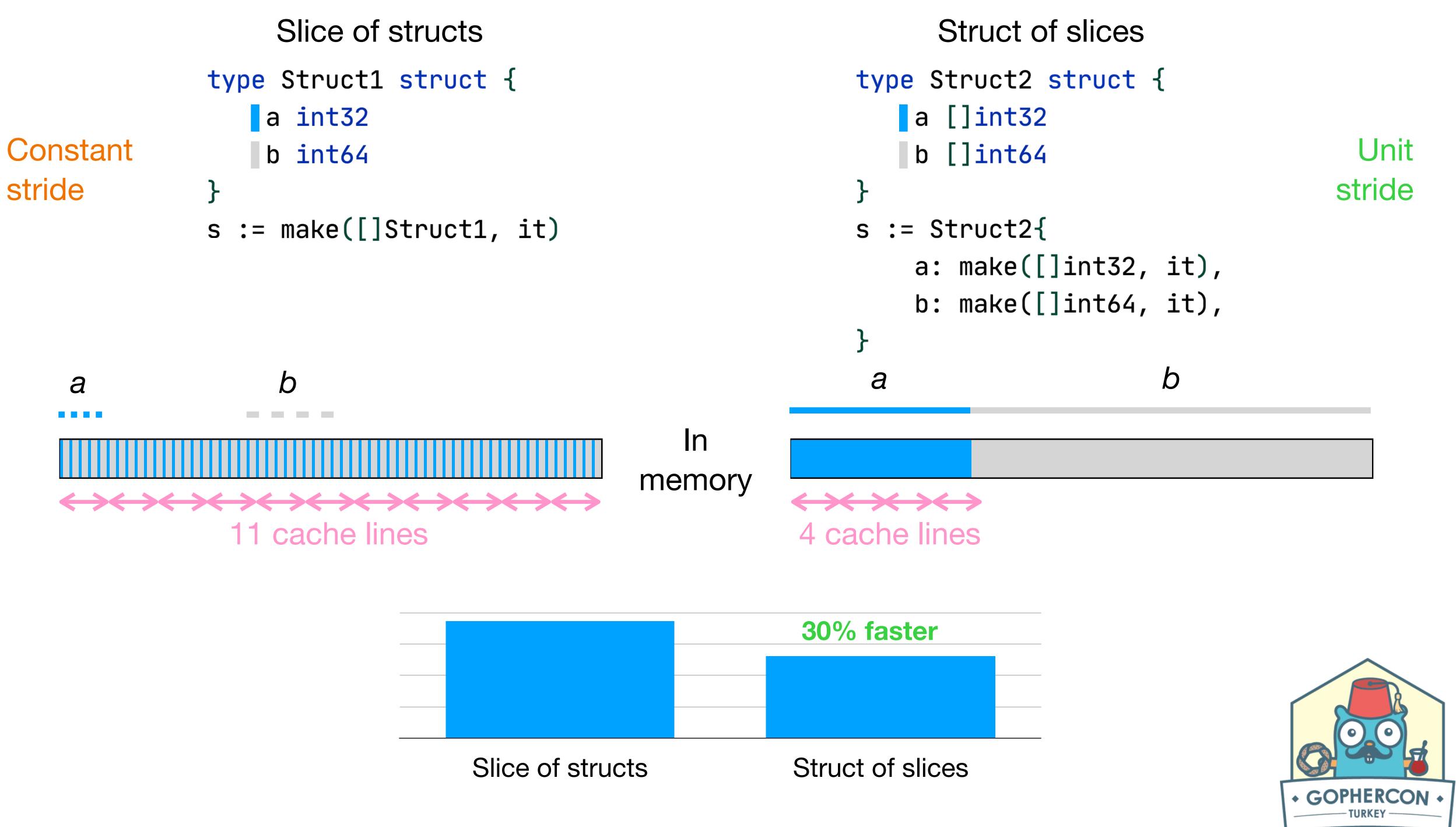
```
s := make([]Struct1, it)
var r int32
b.ResetTimer()
for i := 0; i < b.N; i++ {
    for i := 0; i < it; i++ {
        r = s[i].a
     }
}
result = r</pre>
```

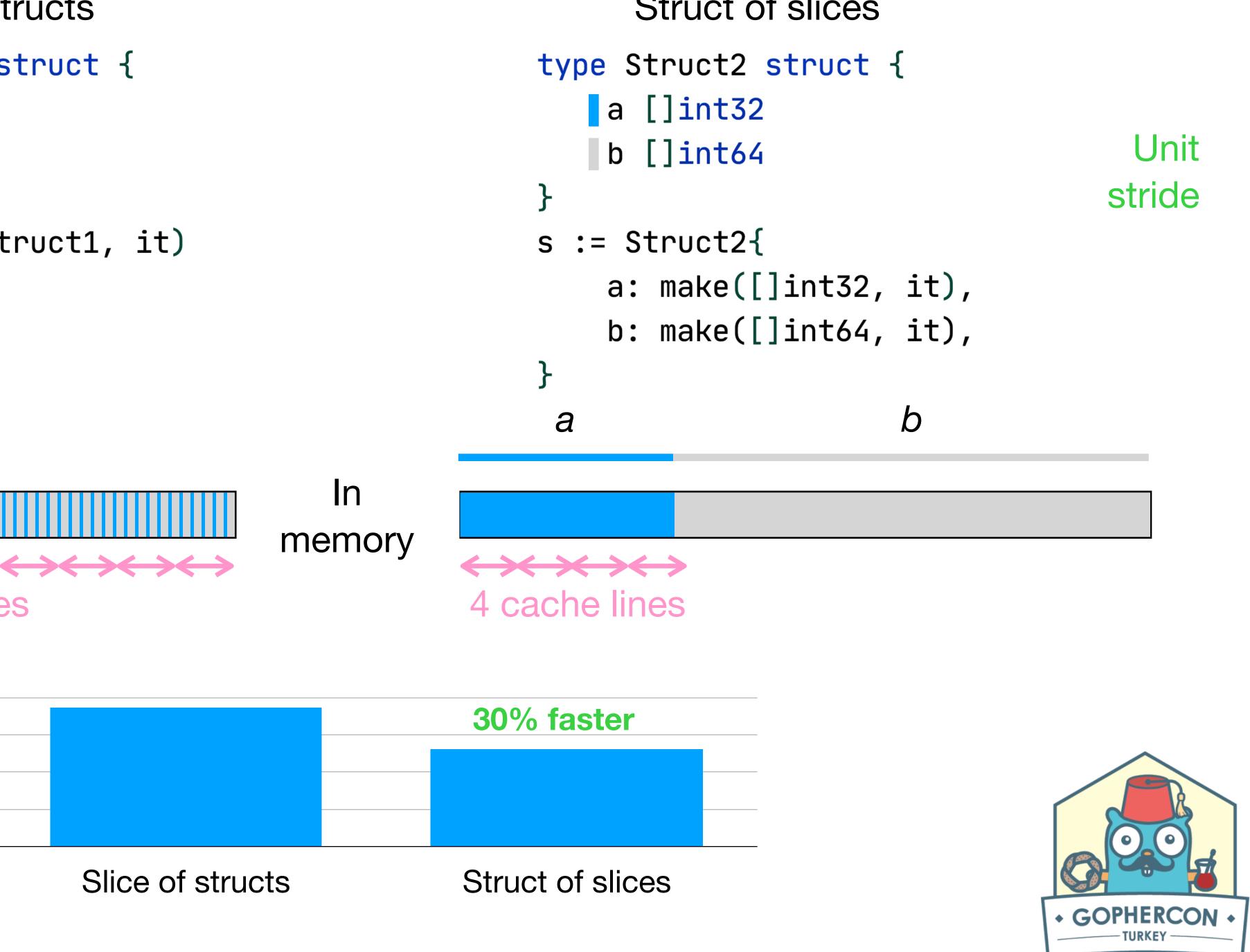
```
type Struct2 struct {
    a []int32
    b []int64
}
```

[func BenchmarkStructureOfSlices(b *testing.B) {

```
s := Struct2{
    a: make([]int32, it),
    b: make([]int64, it),
var r int32
b.ResetTimer()
for i := 0; i < b.N; i++ {</pre>
    for i := 0; i < it; i++ {</pre>
        r = s.a[i]
result = r
```







• A concrete example: Go standard flate package

 Flate is a compression algorithm based on two other algorithms: huffman encoding an LZ77 compression



Go flate package

typ

typ

ype <u>hcode</u> st code, len		<pre>type hcodes struct { code []uint16 len []uint16 }</pre>	
codes	ncoder struct { []hcode []literalNode [17]int32 byLiteral // stored to avoid repeated allocation in generate byFreq // stored to avoid repeated allocation in generate	<pre>type huffmanEncoder struct { codes hcodes fregcache []literalNode bitCount [17]int32 lns byLiteral // stored to avoid lfs byFreq // stored to avoid }</pre>	

https://github.com/golang/go: src/compress/flate/huffman_code.go

• 5 iteration loops on either *hcode.code* or *hcode.len*

• Example:

```
for i := 0; i < numCodegens; i++ {</pre>
for i := 0; i < numCodegens; i++ {</pre>
                                                                          value := uint(w.codegenEncoding.codes.len[codegenOrder[i]])
    value := uint(w.codegenEncoding.codes[codegenOrder[i]].len)
                                                                          w.writeBits(int32(value), nb: 3)
    w.writeBits(int32(value), nb: 3)
                                                                      }
}
```

• Metrics?

Go flate package modified



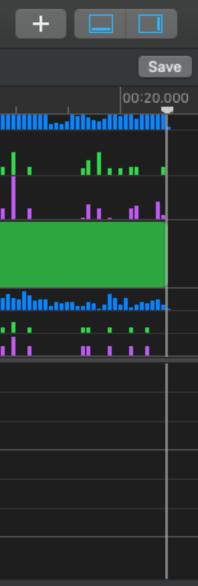
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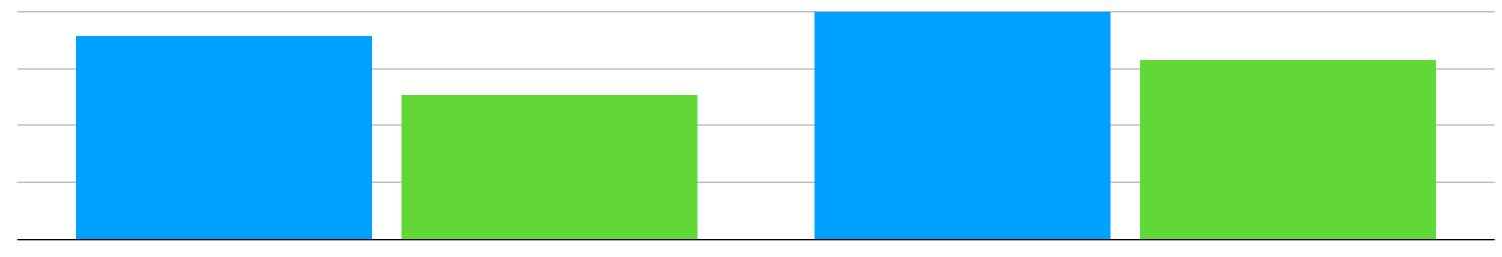
storeHuff

riter).writeBlockHuff der).generate



Go flate package

<pre>type hcode struct { code, len uint16</pre>									
}									
<mark>type</mark> huffma	<pre>type huffmanEncoder struct {</pre>								
codes	[]hcode								
freqca	he []literalNode								
bitCou	t [17]int32								
lns	<pre>byLiteral // stored to avoid repeated allocation in gener</pre>								
lfs	byFreq // stored to avoid repeated allocation in gener								
}									



Encode/Digits/Huffman/1e6

Slice of structs

Go flate package modified

```
type hcodes struct {
           code []uint16
          len []uint16
      }
      type huffmanEncoder struct {
                     hcodes
           codes
          freqcache []literalNode
          bitCount [17]int32
erate
                    byLiteral // stored to avoid repeated allocation in generate
          lns
erate
                               // stored to avoid repeated allocation in generate
          lfs
                    byFreq
```

Encode/Newton/Huffman/1e6



Struct of slices







• I can design algorithms to leverage CPU caches

I can also organise my data to get the most value out of cache lines

• **Unit stride** > Constant stride > Non-unit stride



CPU Architecture Locality of Reference **Data-Oriented Design** Caching Pitfall Concurrency



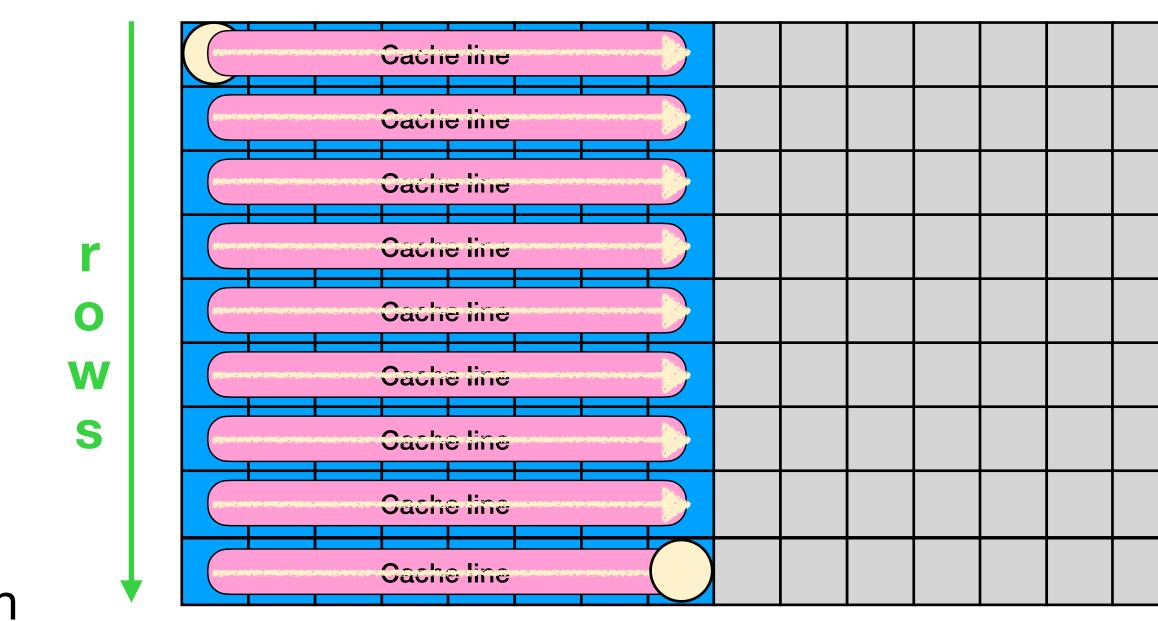
- Two-dimensional array of int64s 64 bytes cache line (8 elements)
- Traverse each row multiple times the first
 8 columns only

```
for 0..k {
    for i in 0..rows {
        for j in 0..8 {
            sum += a[i][j]
        }
    }
}
```

- rows is small enough so that each line should fit in the cache
- The execution time depends on **n** (?)
- Depending on n, the execution can be up to 100% slower

n columns (variable)

8 int64s



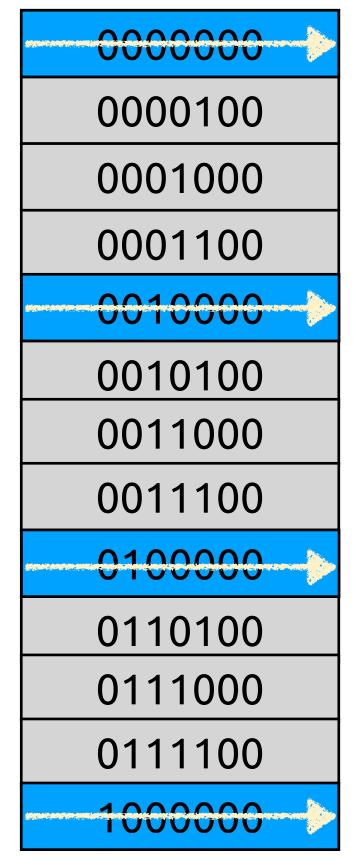




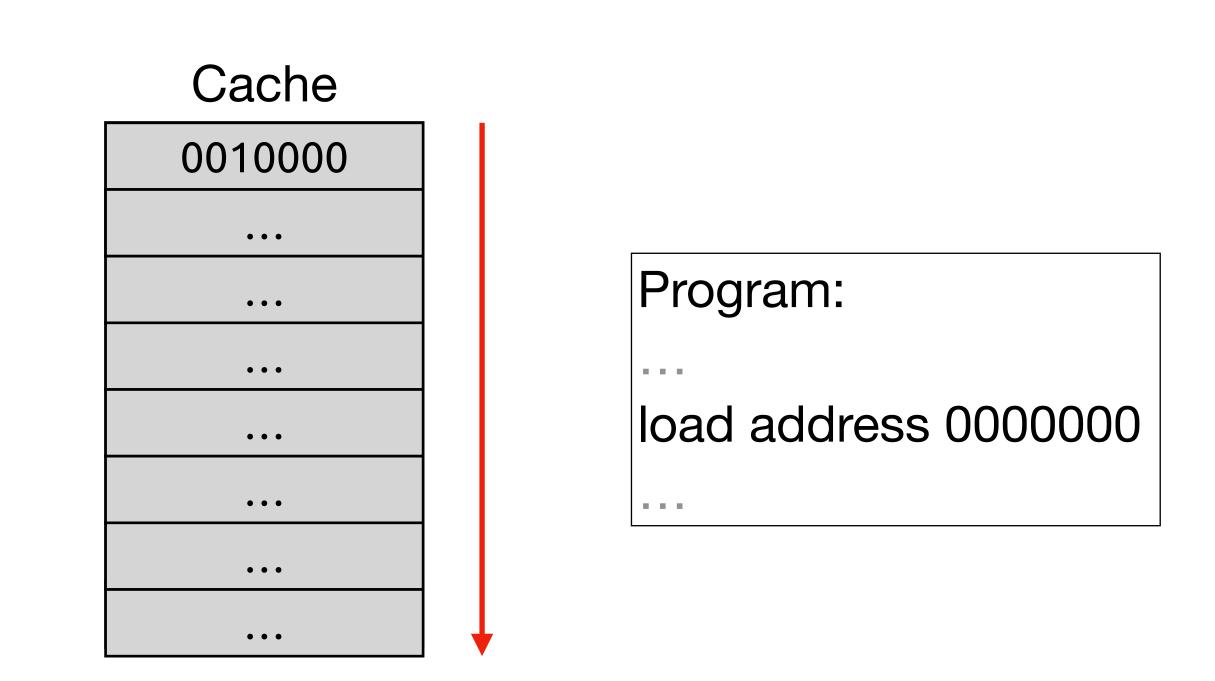
Matrix in memory

A block is referenced by an address

We want to iterate on each **blue block**

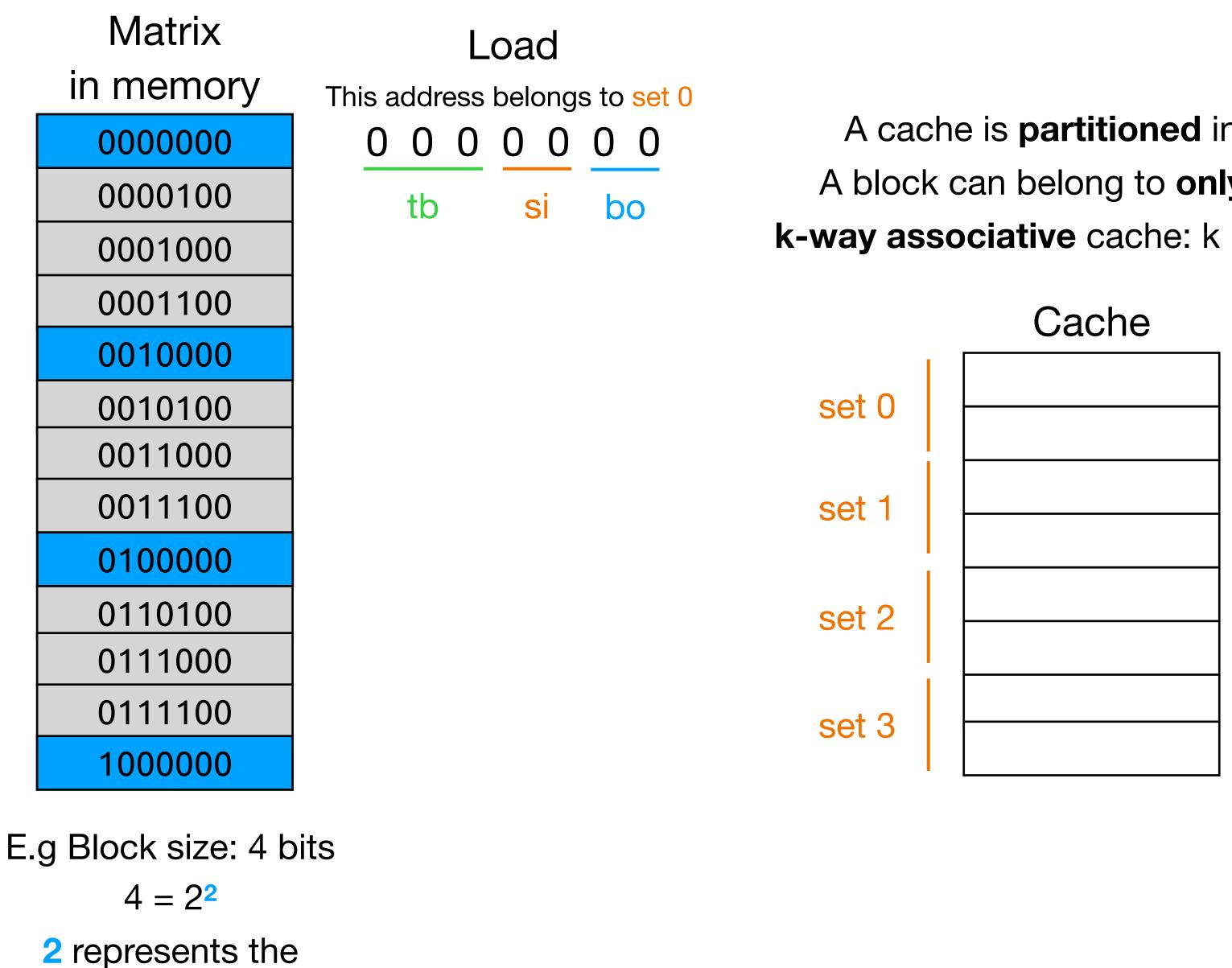


- address is present
- Example on an Intel Core i5-7300 L1D: we need to iterate on 512 lines
- Solution: partitioning



• In a fully associative cache, we may have to traverse the whole cache to check if an

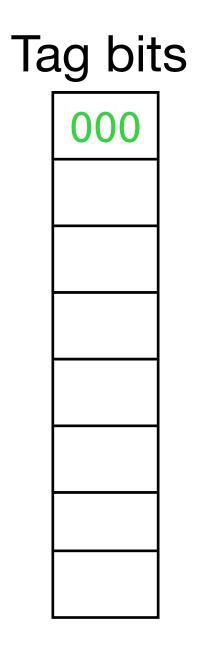




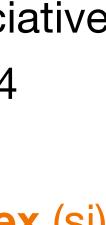
block offset (bo)

A cache is **partitioned** into **sets** A block can belong to **only one** set k-way associative cache: k lines per set E.g. 8 lines, 2-way associative nb of sets = 8 / 2 = 4 $4 = 2^{2}$

2 represents the set index (si)

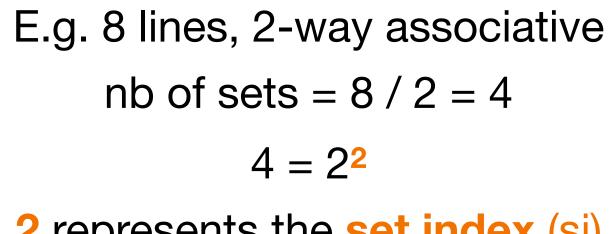




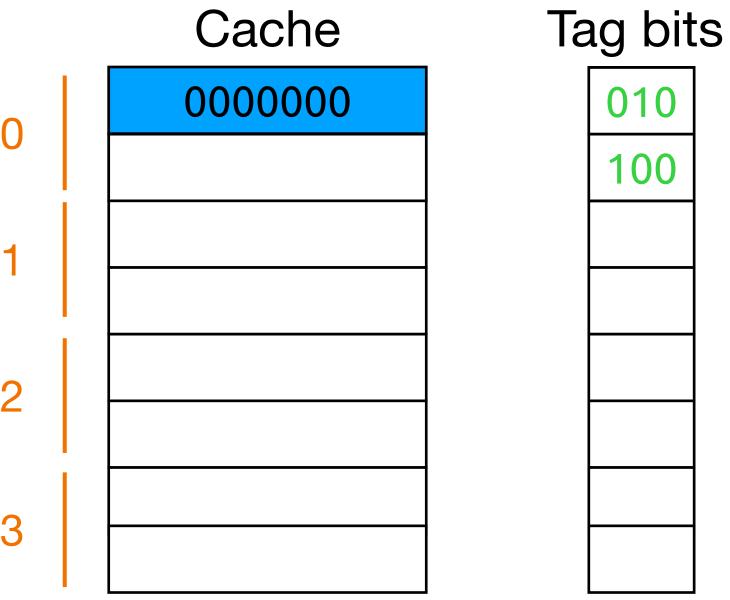


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	0000100		tb		si	bo	A blog	
	0001000						k-way a	
	0001100							
	0010000	0	0	1	0 0	0 0		
	0010100		tb		si	bo	set 0	
	0011000							
	0011100						set 1	
	0100000	0	1	0	0 0	0 0		
	0110100		tb		si	bo	set 2	
	0111000							
	0111100						set 3	
	1000000	1	0	0	0 0	0 0		
F	g Block size: 4 bit	c	tb		si	bo		
L .	$4 = 2^2$	3					The distribution	
	2 represents the						It will generate	
	block offset (bo)						~	
							This consta	

ache is **partitioned** into sets ock can belong to **only one** set associative cache: k lines per set



2 represents the set index (si)



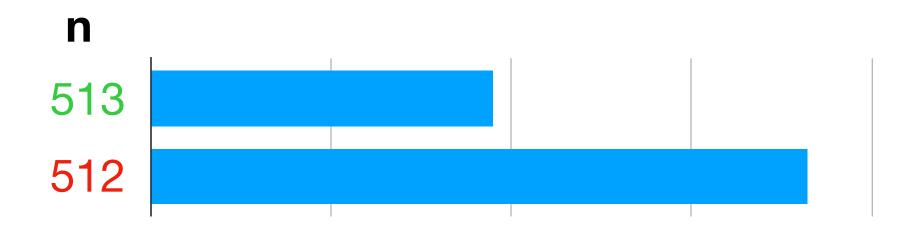
ion is not even, we used **only one set**

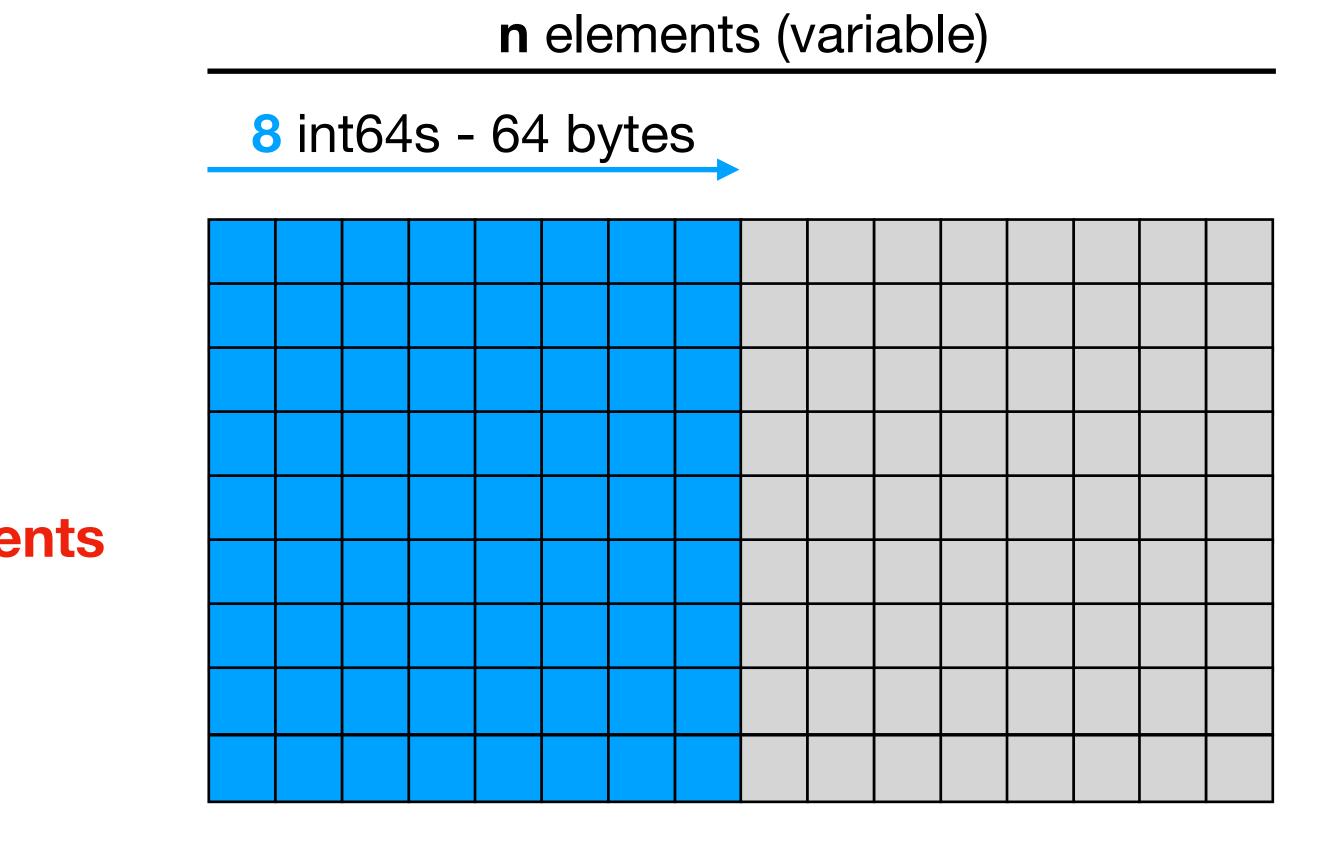
te a lot of cache misses (conflict miss)

ant stride is called the critical stride



- Critical stride = nb sets x cache line size
- Example with an Intel Core i5-7300:
 - Cache line = 64 bytes
 - 32 KB, 8-way set associative, 64 sets
 - Critical stride = $64 \times 64 = 4 \text{ KB}$
- We reach a critical stride with n = **512** elements
- If n = 512, we are going to use 1 set only









CPU caches are partitioned

Critical stride

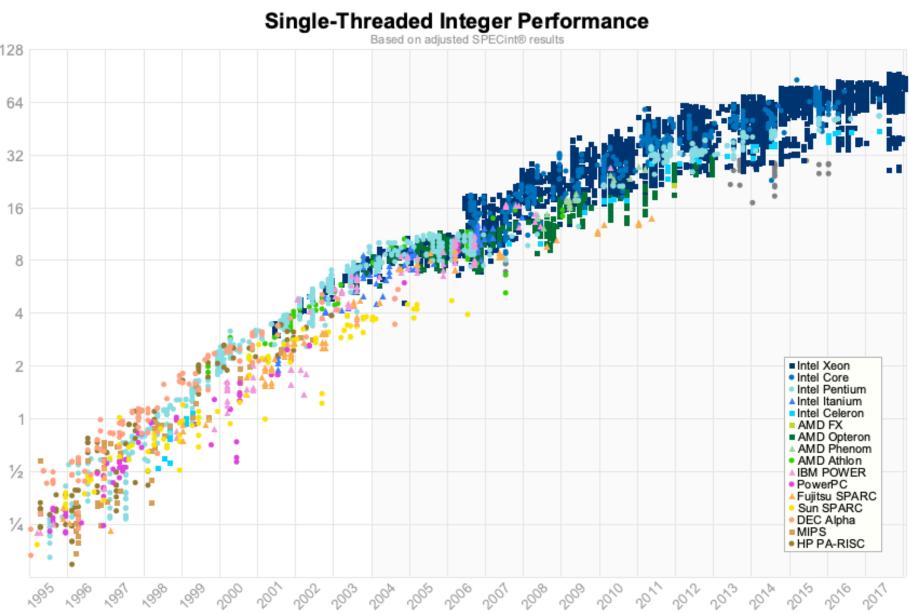
• Depending on my data, my application can occupy a fraction of the cache only



CPU Architecture Locality of Reference **Data-Oriented Design** Caching Pitfall Concurrency



Why Concurrency?



- Instead of focusing on clock speed, vendors focus on multicores and hyperthreading architectures
- The free lunch is over Herb Sutter, 2005
- We cannot rely solely on the hardware to make our programs faster **Concurrency** is the next major revolution in how we write software



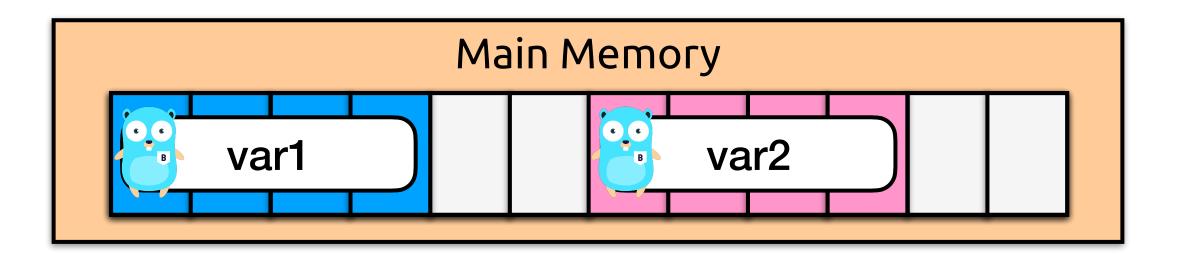
```
type Struct struct {
    n int
var <mark>result</mark> int
func BenchmarkIteration(b *testing.B) {
    structA := Struct{} // Initialization
    structB := Struct{} // Initialization
    wg := sync.WaitGroup{}
    b.ResetTimer()
    for i := 0; i < b.N; i++ {</pre>
        wg.Add( delta: 2)
        go func() { // Spin up first goroutine
             for j := 0; j < iteration; j++ {</pre>
                 structA.n += j
             }
             wg.Done()
         }()
        go func() { // Spin up second goroutine
             for j := 0; j < iteration; j++ {</pre>
                 structB.n += j
             }
             wg.Done()
        wg.Wait() // Wait
```

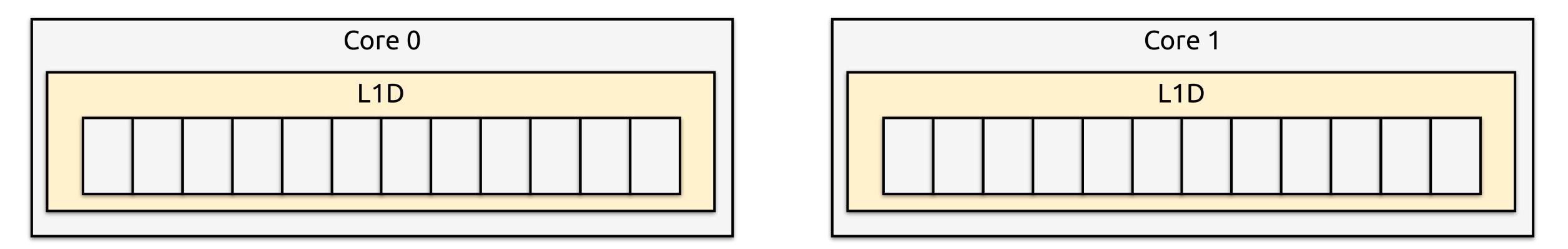
}

result = structA.n + structB.n // Aggregate

Race-free implementation!

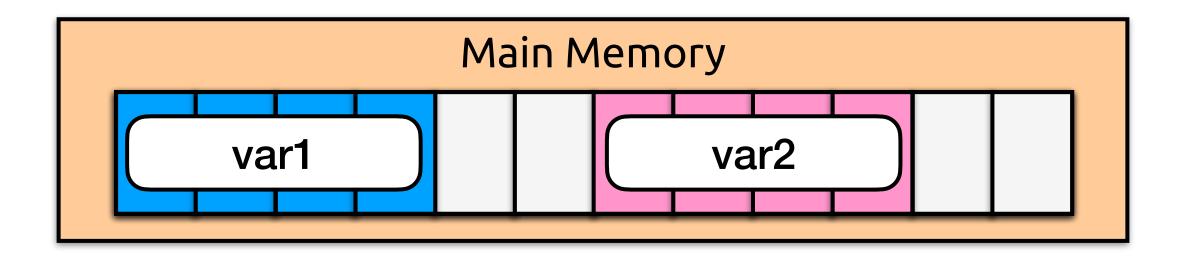


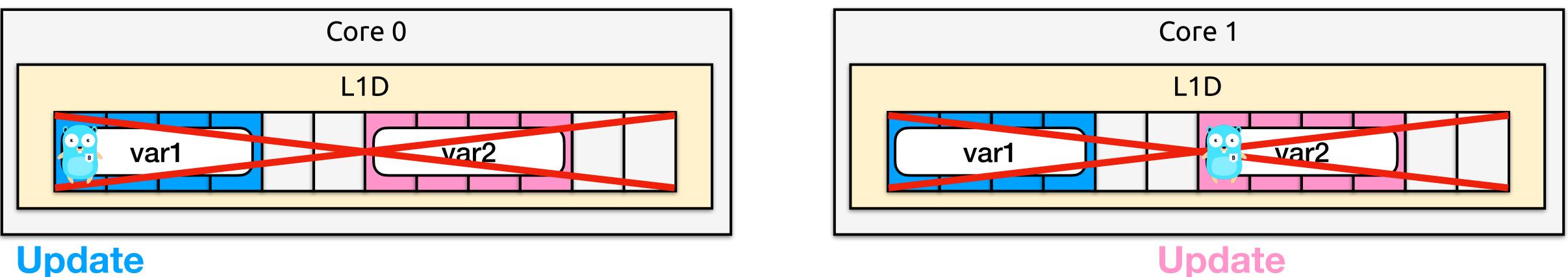




- What if both goroutines want to update their own lines
- The CPU must guarantee cache coherency
- MESI protocol (Modified, Exclusive, Shared, Invalid) ullet







Update

- Why does it matter?
- False sharing a cache line is shared across two cores with at least one goroutine being a writer
- Sharing memory is an **illusion**



```
type Struct struct {
    n int
}
var <mark>result</mark> int
func BenchmarkIteration(b *testing.B) {
    structA := Struct{} // Initialization
    structB := Struct{} // Initialization
    wg := sync.WaitGroup{}
    b.ResetTimer()
    for i := 0; i < b.N; i++ {</pre>
        wg.Add( delta: 2)
        go func() { // Spin up first goroutine
            for j := 0; j < iteration; j++ {</pre>
                 structA.n += j
             }
            wg.Done()
        }()
        go func() { // Spin up second goroutine
             for j := 0; j < iteration; j++ {</pre>
                 structB.n += j
             }
            wg.Done()
        }()
        wg.Wait() // Wait
        result = structA.n + structB.n // Aggregate
}
```

structA.n and structB.n belongs to the same cache line



False Sharing

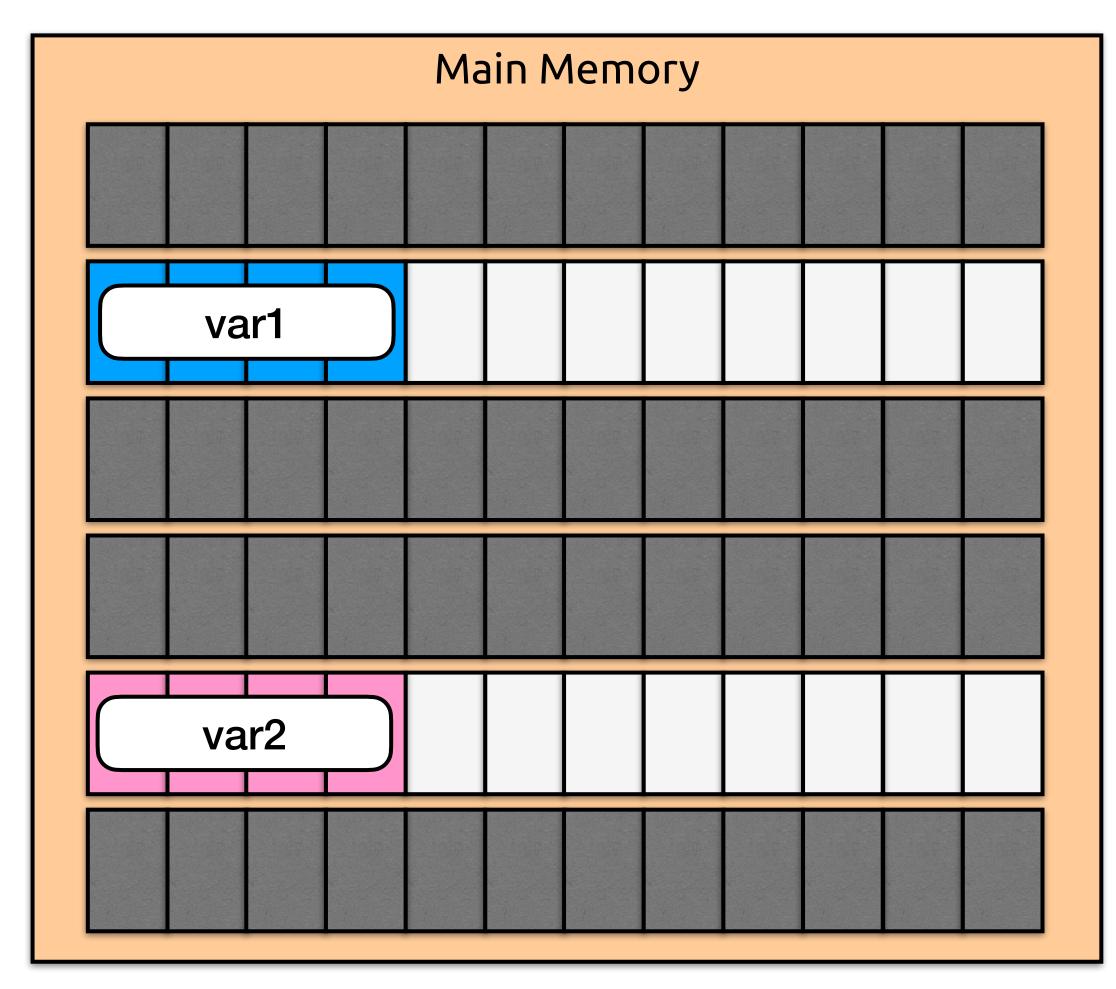
- How to prevent false sharing?
- Solution 1: Do not communicate by sharing memory; instead, share memory by communicating





False Sharing

- How to prevent false sharing?
- Solution 2: padding



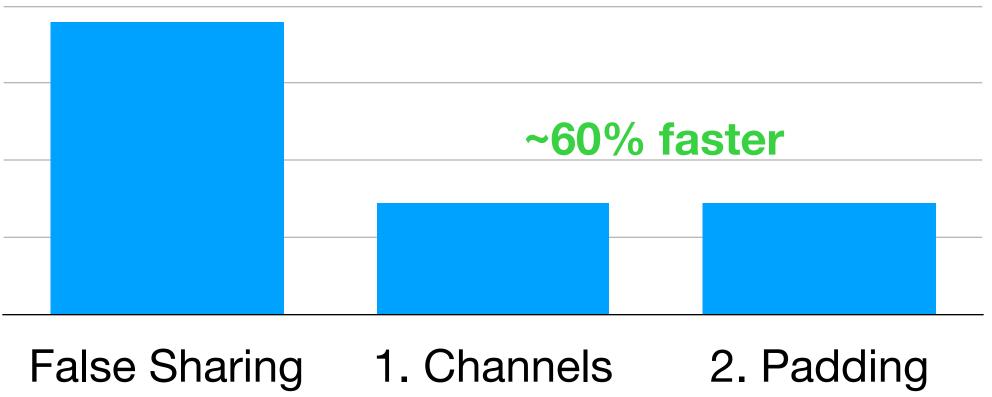
```
type PaddedStruct struct {
   _ cpu.CacheLinePad // 64 bytes
   n int
   _ cpu.CacheLinePad // 64 bytes
}
```

```
func BenchmarkIterationWithPadding(b *testing.B) {
    structA := PaddedStruct{} // Initialization
    structB := PaddedStruct{} // Initialization
    wg := sync.WaitGroup{}
    b.ResetTimer()
    for i := 0; i < b.N; i++ {</pre>
        wg.Add( delta: 2)
        go func() { // Spin up first goroutine
            for j := 0; j < iteration; j++ {</pre>
                 structA.n += j
            wg.Done()
        }()
        go func() { // Spin up second goroutine
            for j := 0; j < iteration; j++ {</pre>
                 structB.n += j
            wg.Done()
        }()
        wg.Wait() // Wait
```



False Sharing

• Let's compare the results:



- Padding is hard Dave Cheney
- Sometimes, padding is necessary. E.g. we are obliged to share memory and we want to prevent false sharing (library, etc.).



Conclusion



3 Main Takeaways

- Sharing memory is an illusion
- A code that looks perfectly valid might still be **problematic** at CPU level:
 - Caching distribution
 - False sharing
- We can help the CPU with locality of reference and predictability (algorithms & data structures)

What else?

- Watch out for premature:
 - Optimisations
 - Concurrency
- Mechanical sympathy goes beyond the very scope of CPUs







