Mechanical Sympathy in Go

You don’t have to be an engineer to be a racing driver,
but you do have to have **mechanical sympathy**

Sir Jackie Stewart - three-time F1 world champion

Mechanical Sympathy Applied to IT

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- Yet, having an understanding of how does a machine work can make us a **better developer** (algorithms, data structures)

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- As developers, we **don’t need** to be hardware engineers
- Yet, having an understanding of how does a machine work can make us a **better developer** (algorithms, data structures)

- Today: How to be a **better Go developer** by understanding how CPUs are working

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Teiva Harsanyi

teivah

Software Engineer - Beat

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HIRING

SOFTWARE ENGINEERS

ON CUTTING-EDGE TECHNOLOGIES

DISCOVER YOUR NEXT CHALLENGE
IN **AMSTERDAM, ATHENS** OR **REMOTE**

BEAT

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CPU Architecture

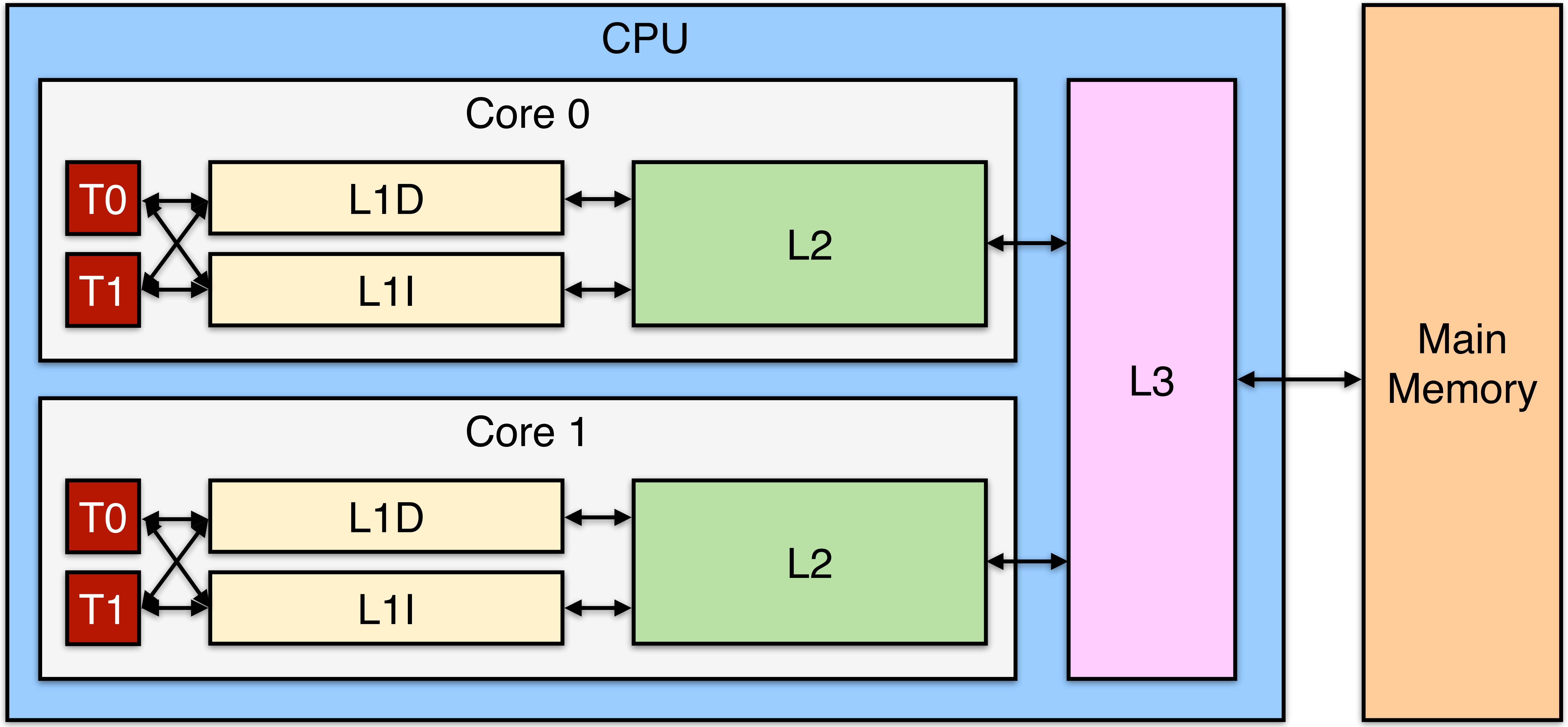
Locality of Reference

Data-Oriented Design

Caching Pitfall

Concurrency

CPU Architecture - Intel Core i5-7300



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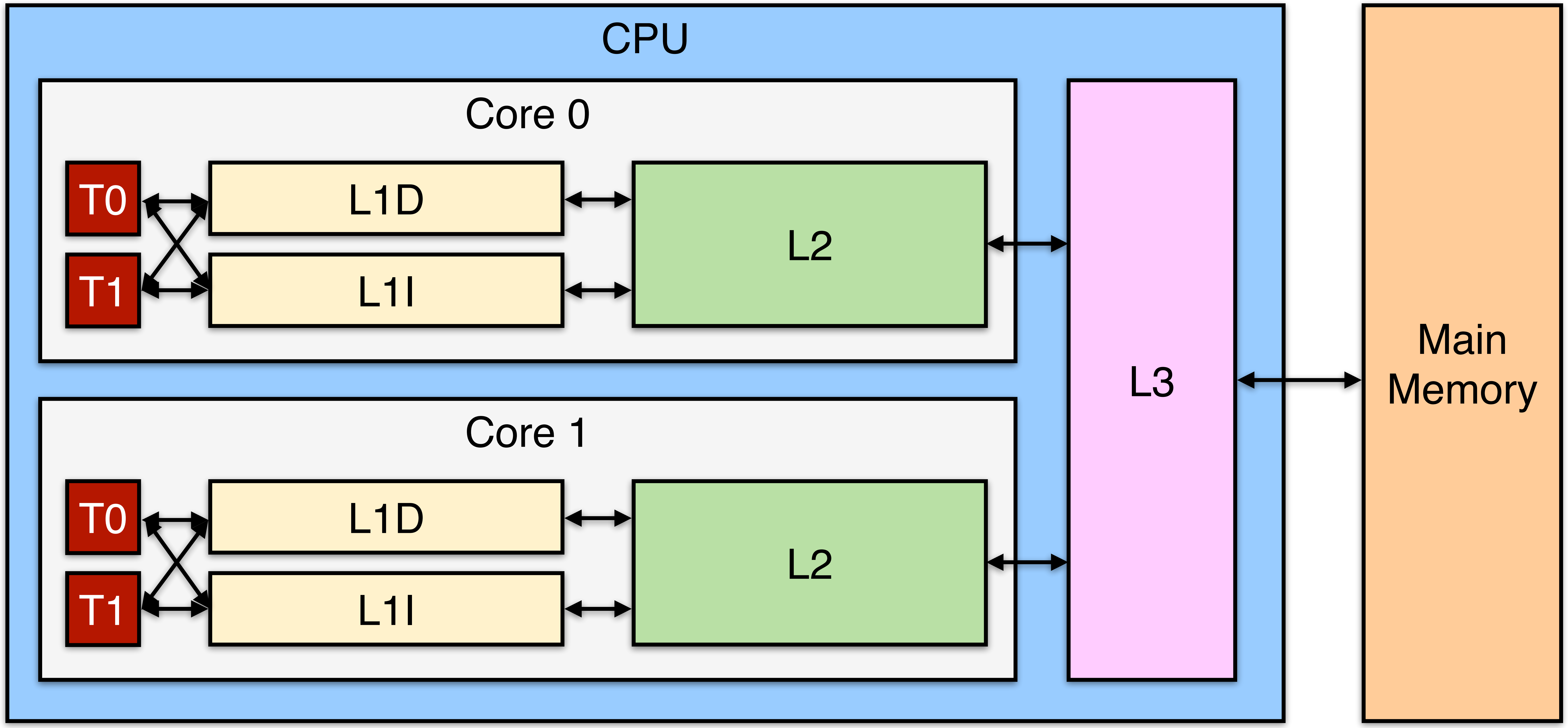

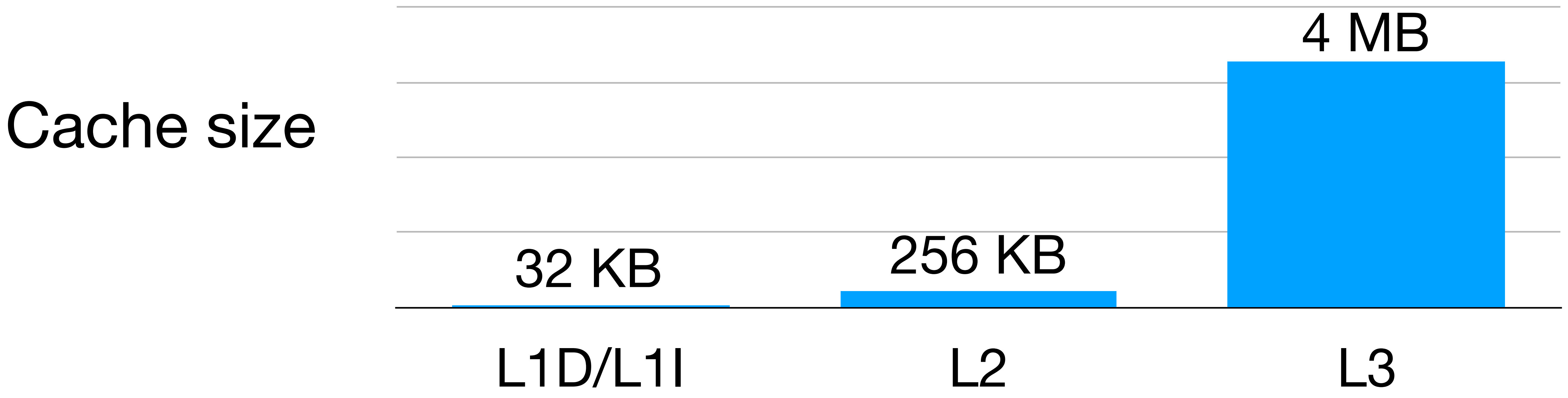

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L1	~1 ns
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As a developer,
I would like my application to leverage CPU caches

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Spatial Locality — **Nearby memory locations** will be referenced in a near future

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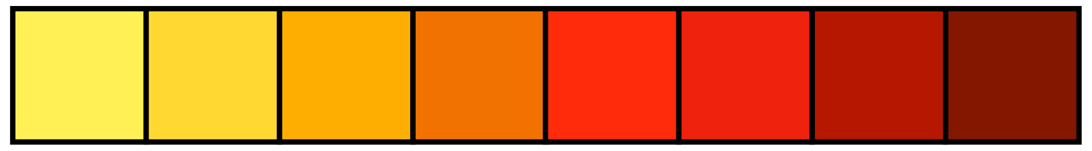

Slice (in our heads)

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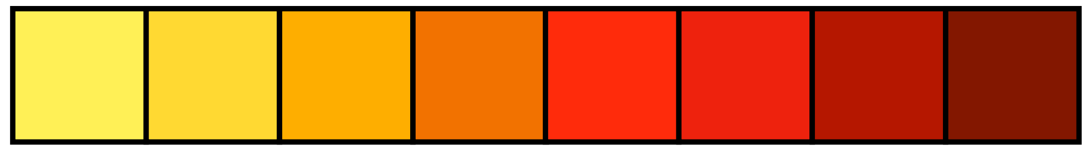

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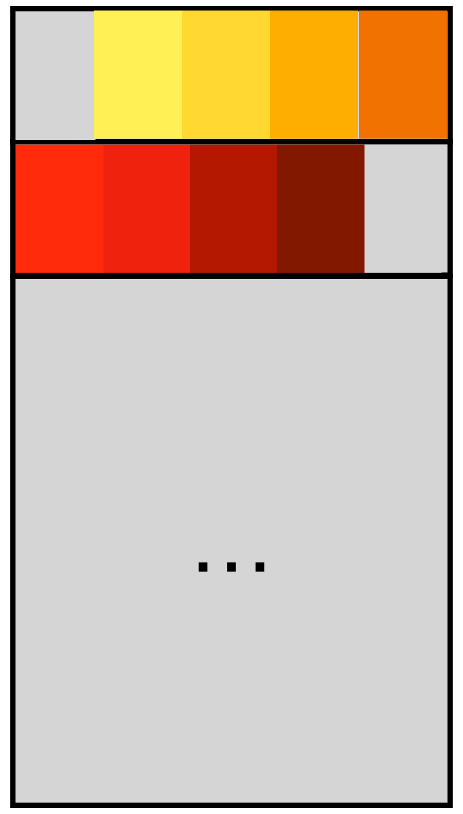

Matrix (main memory)

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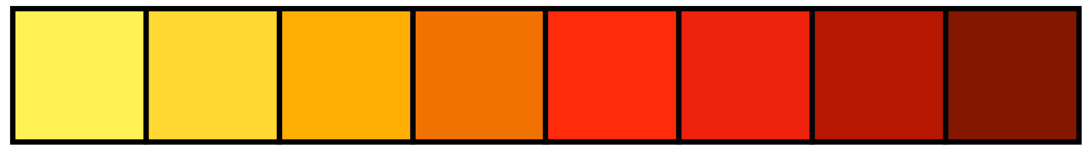

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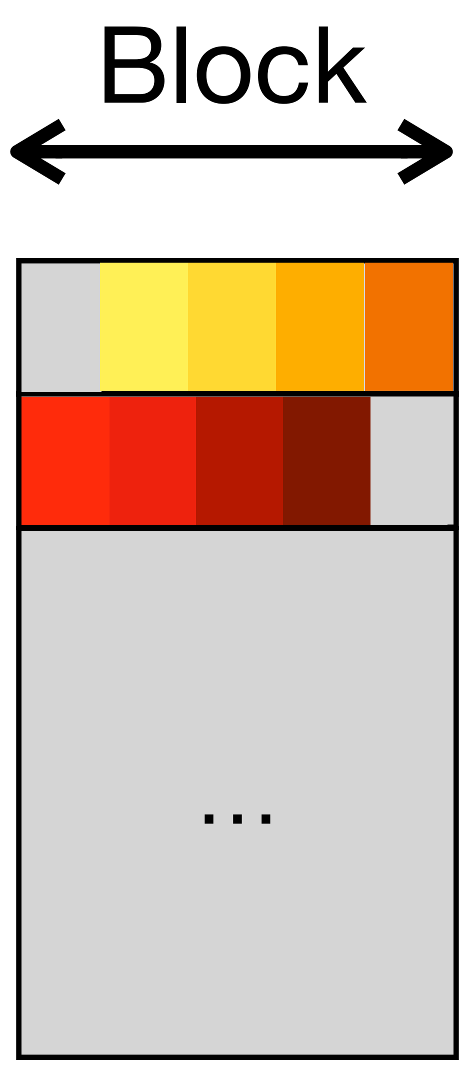

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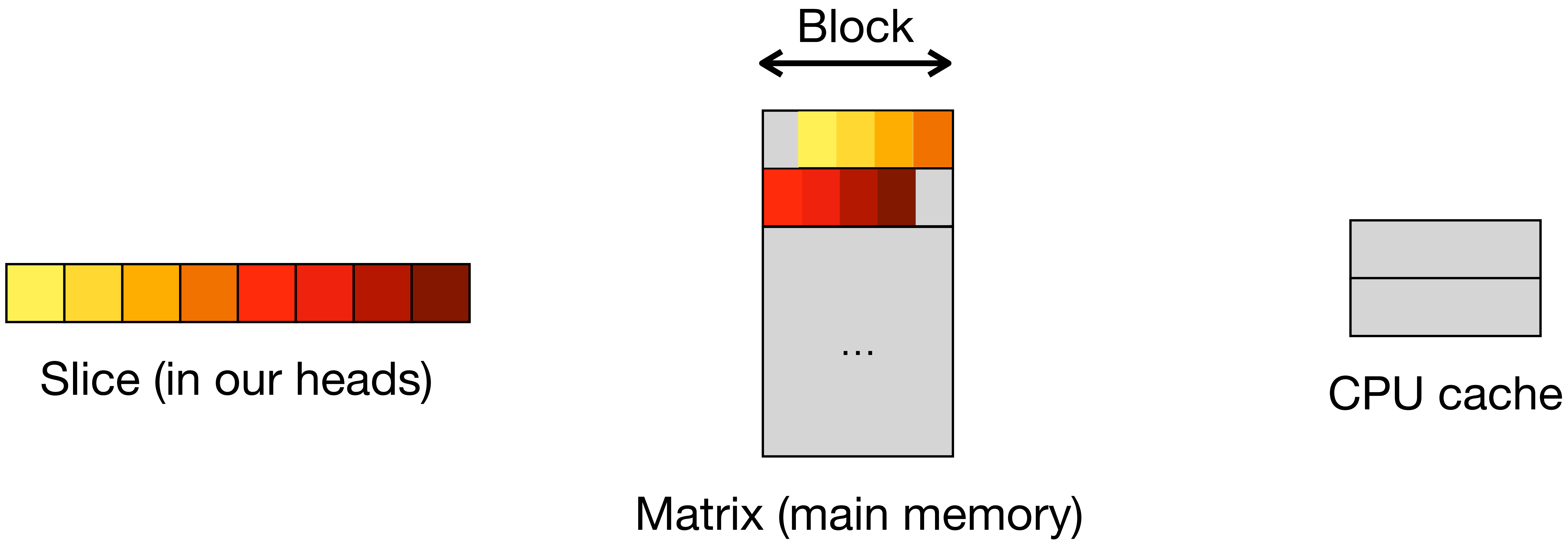

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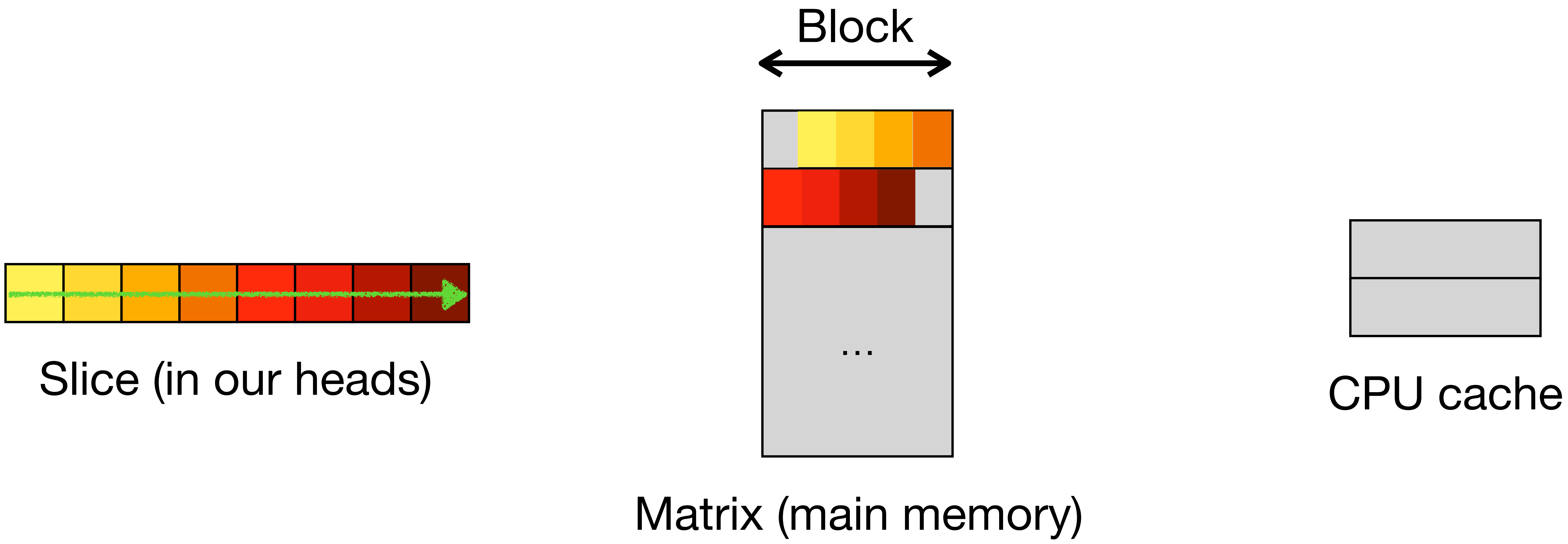

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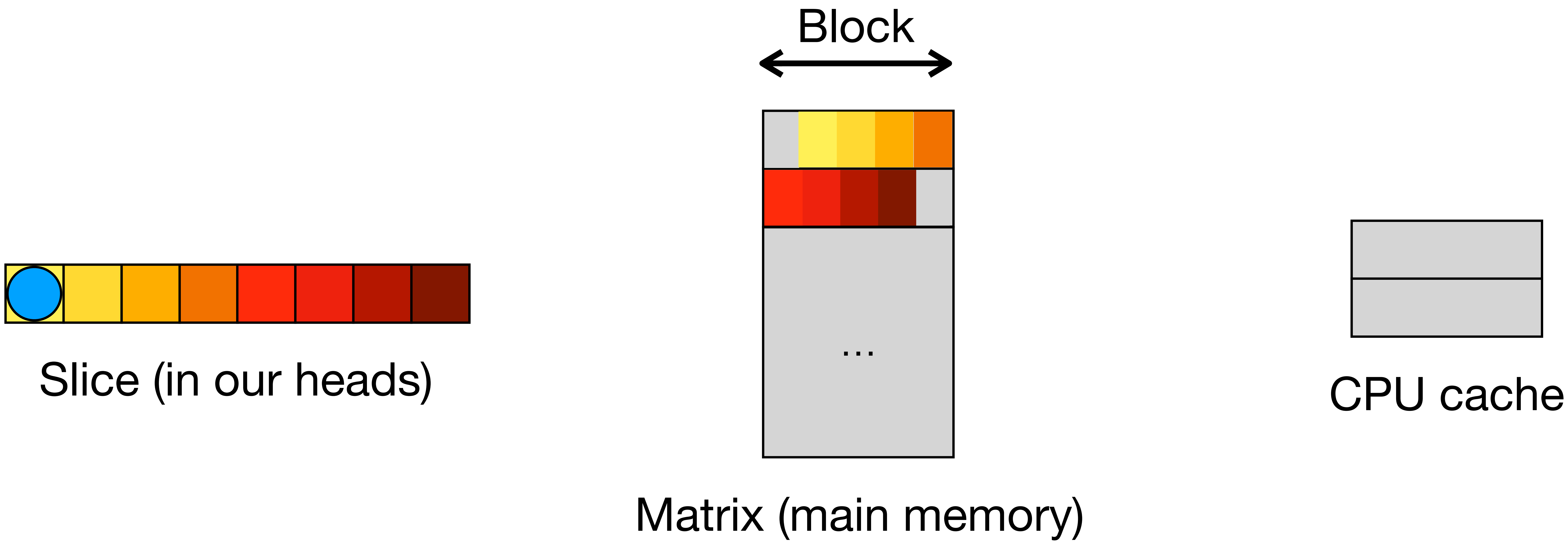

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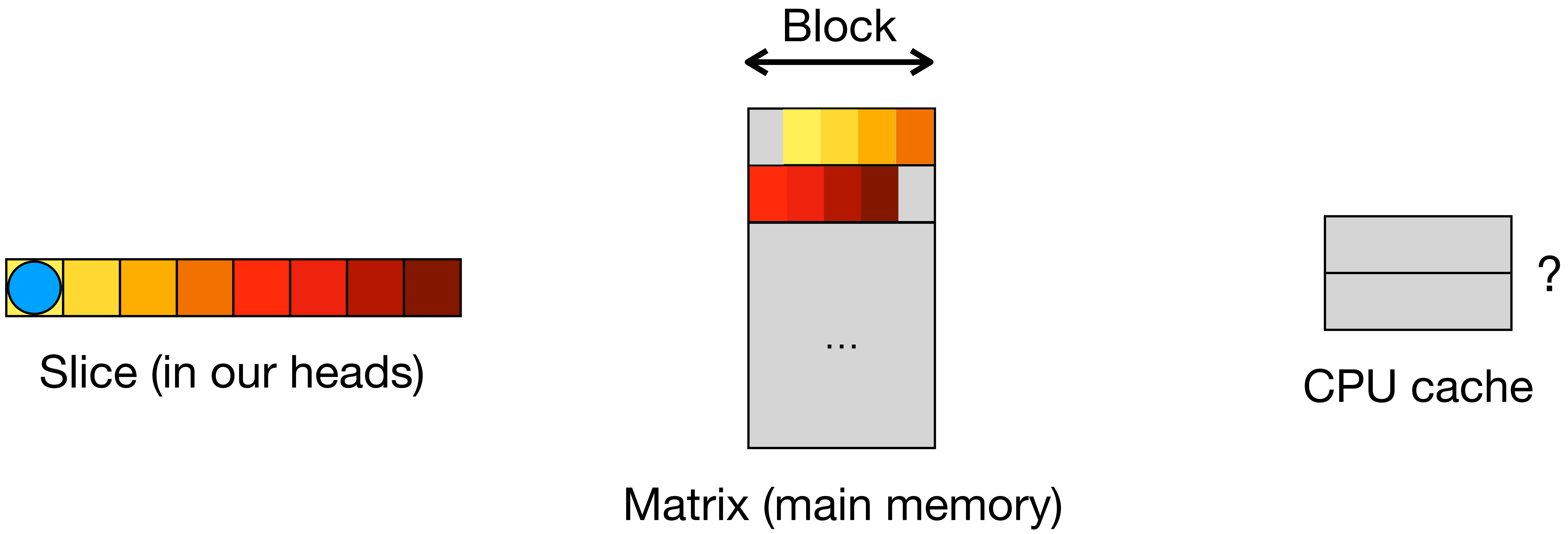

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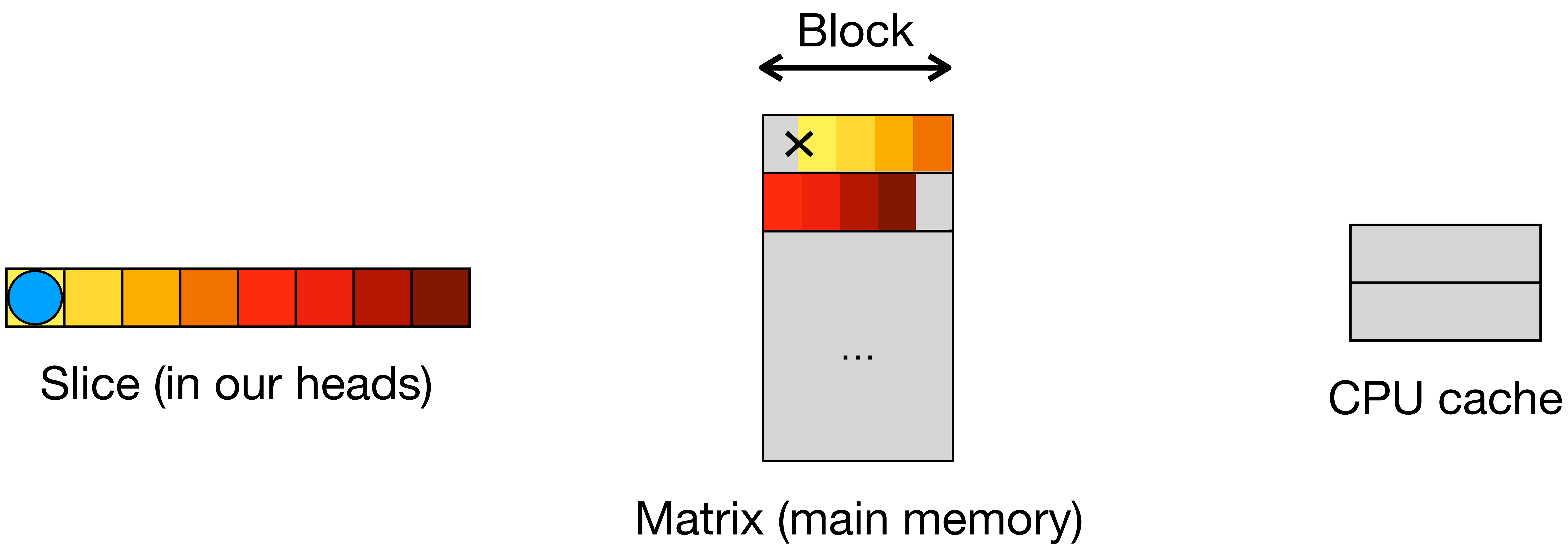

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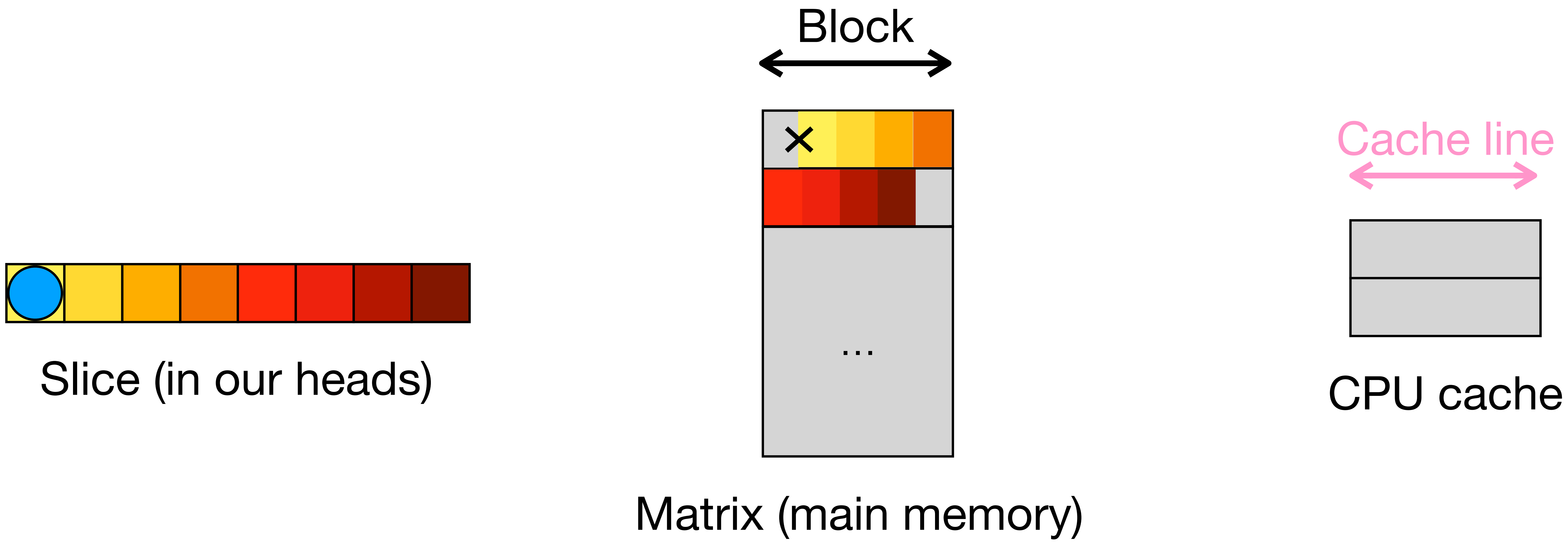

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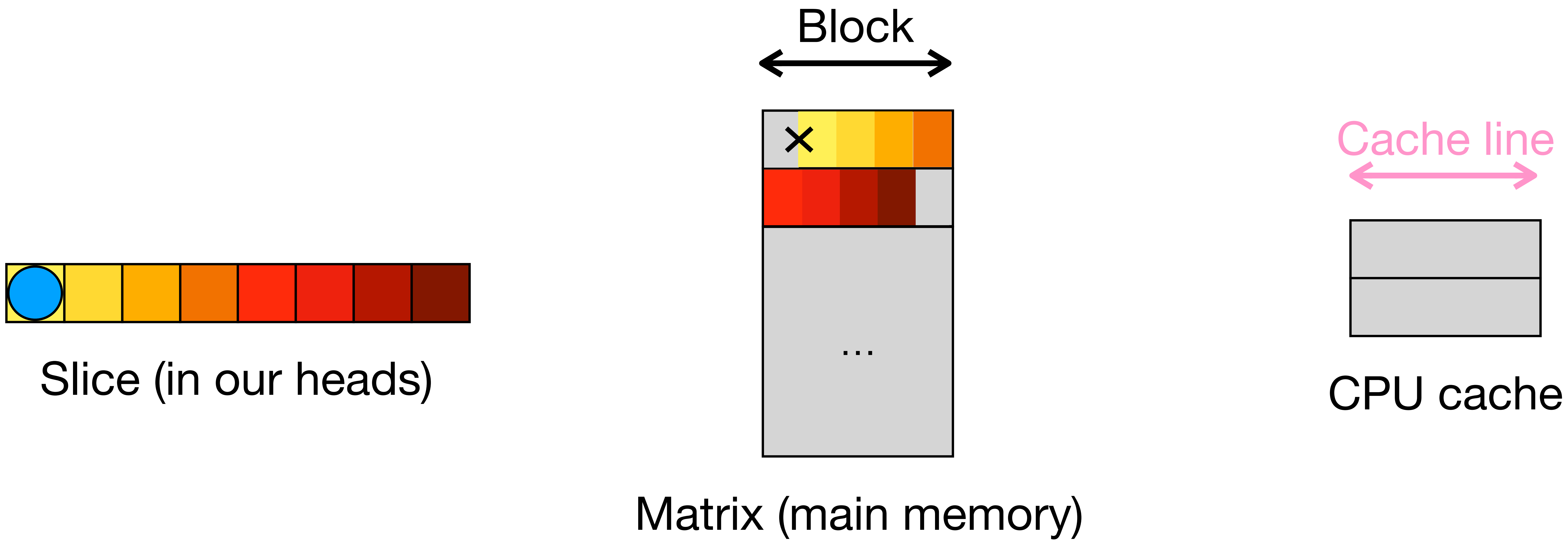

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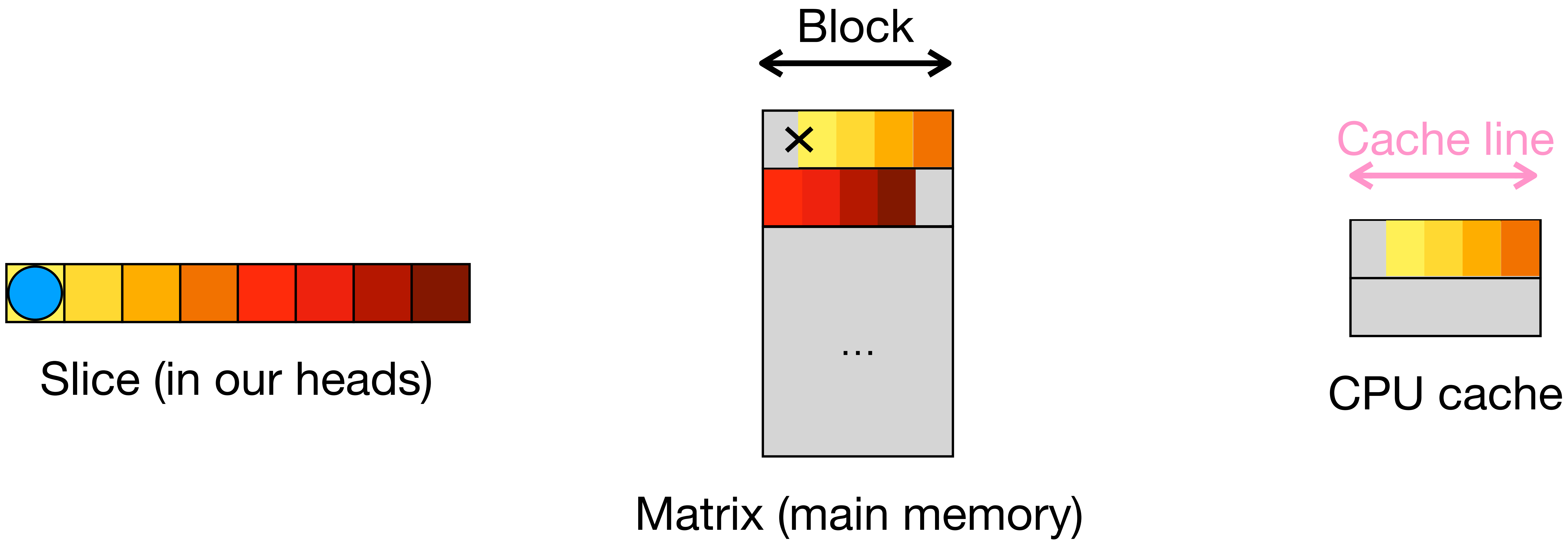

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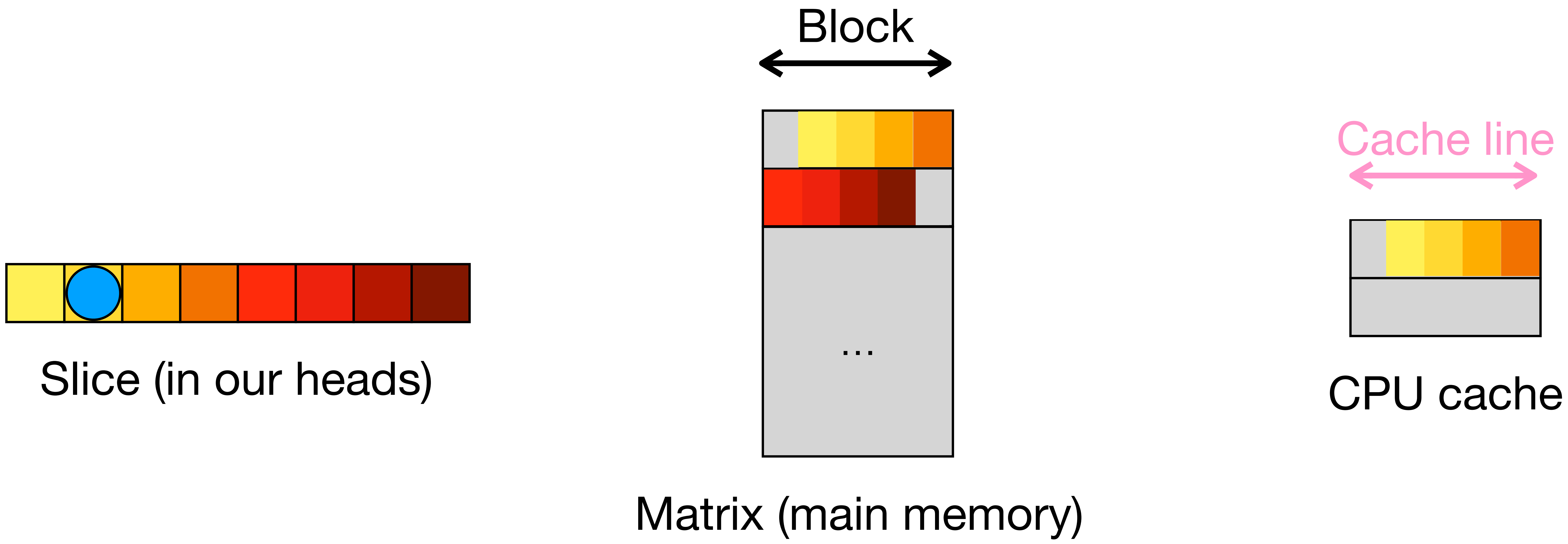

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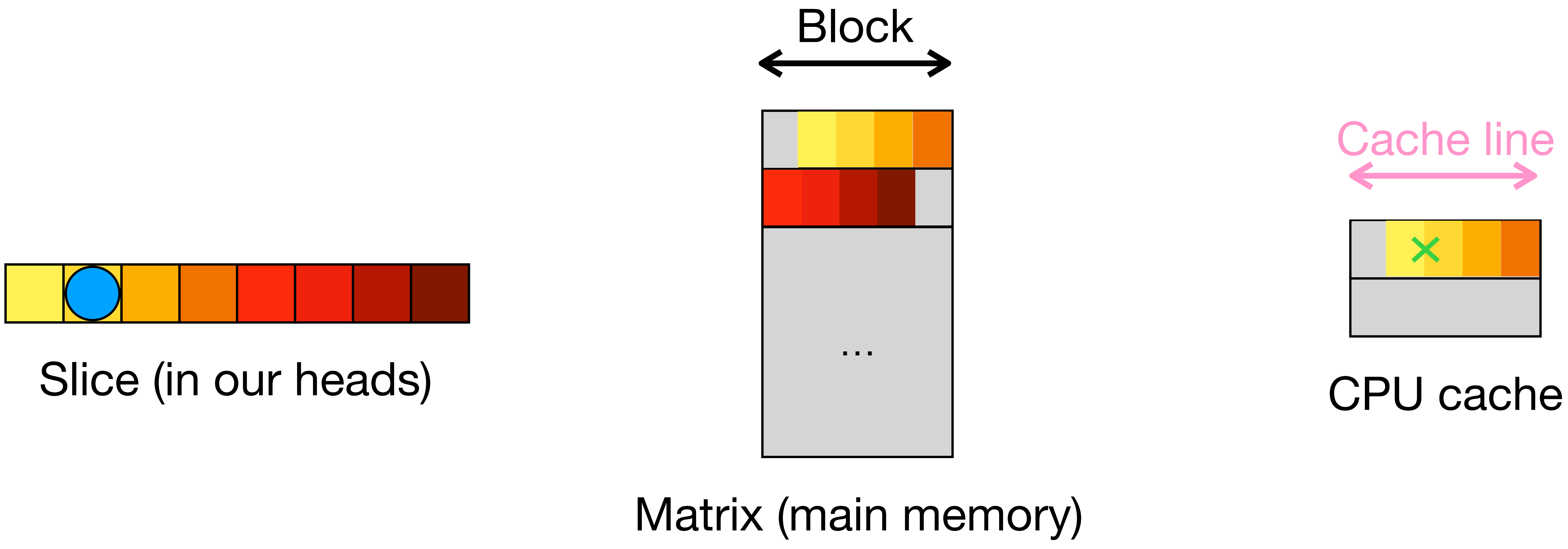

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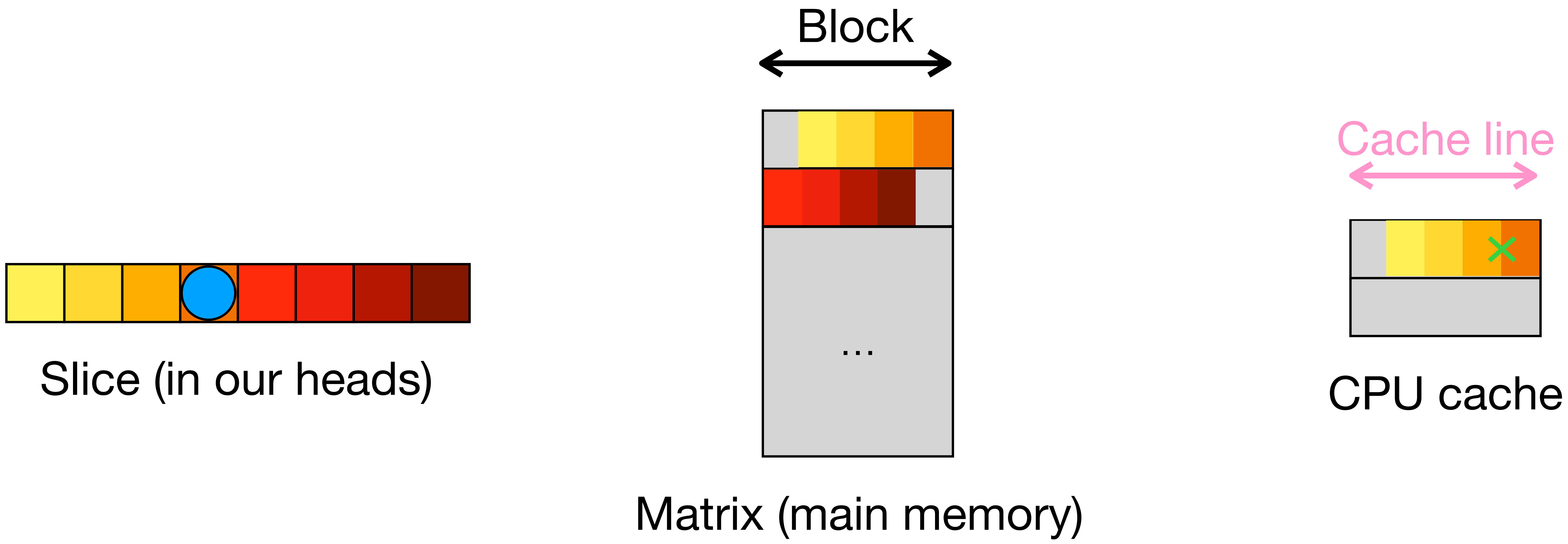

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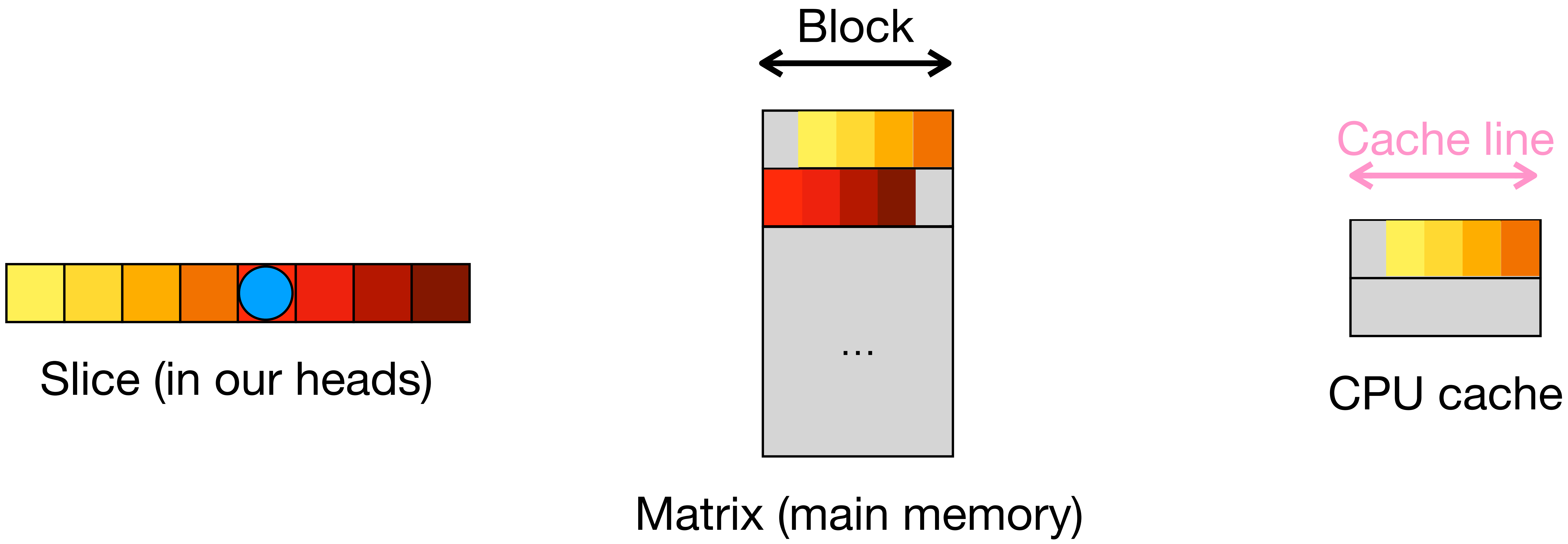

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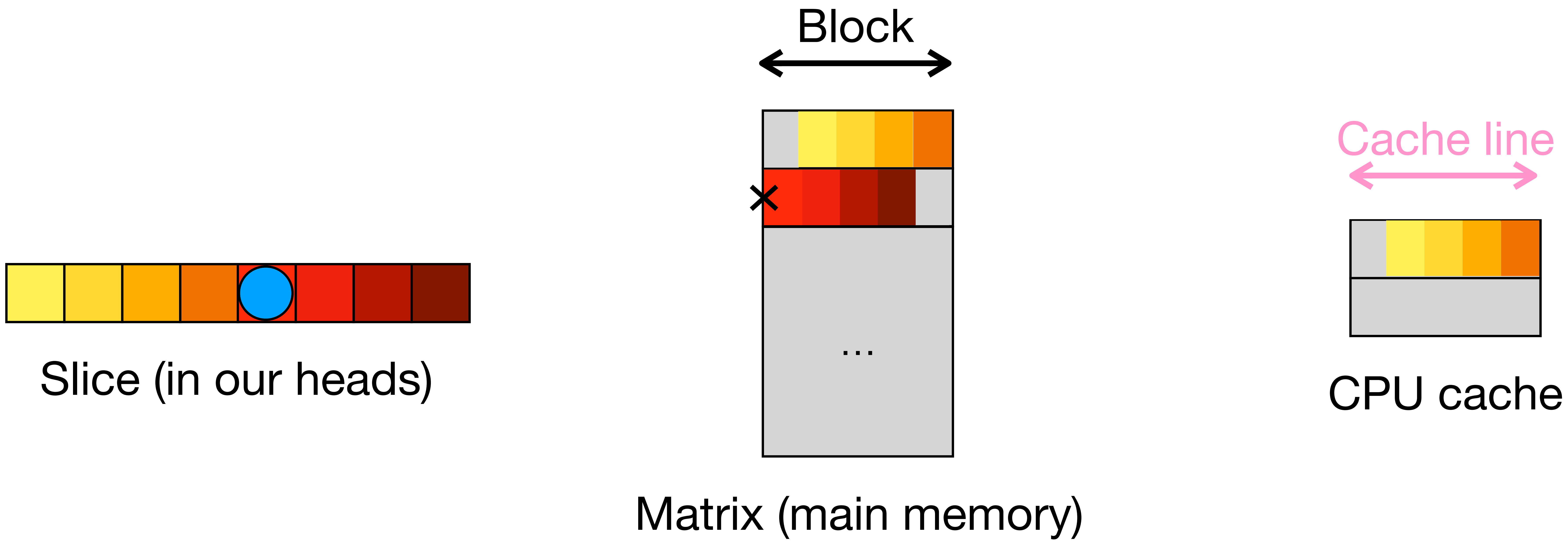

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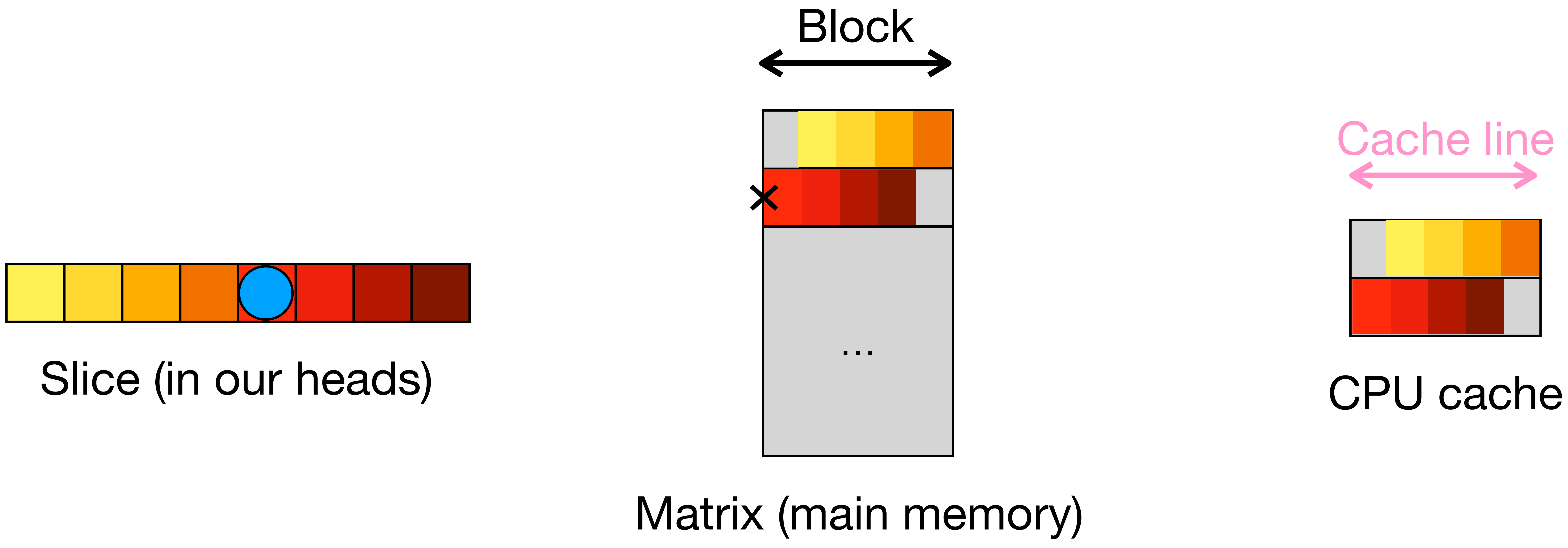

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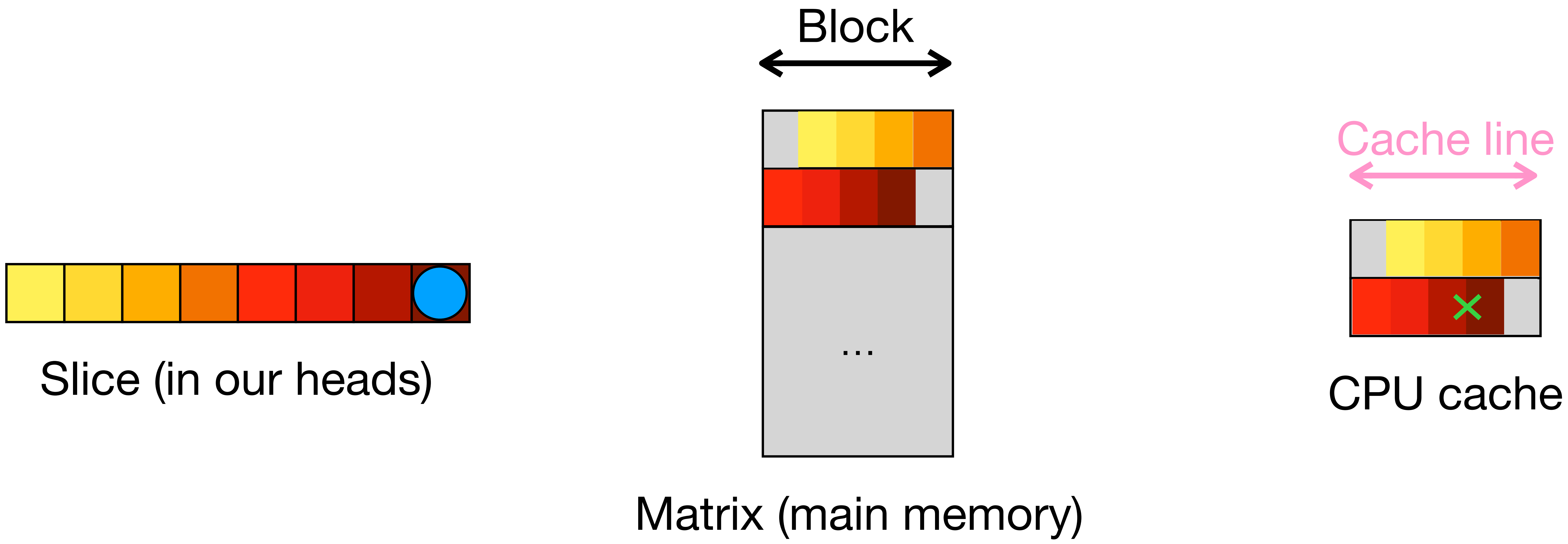

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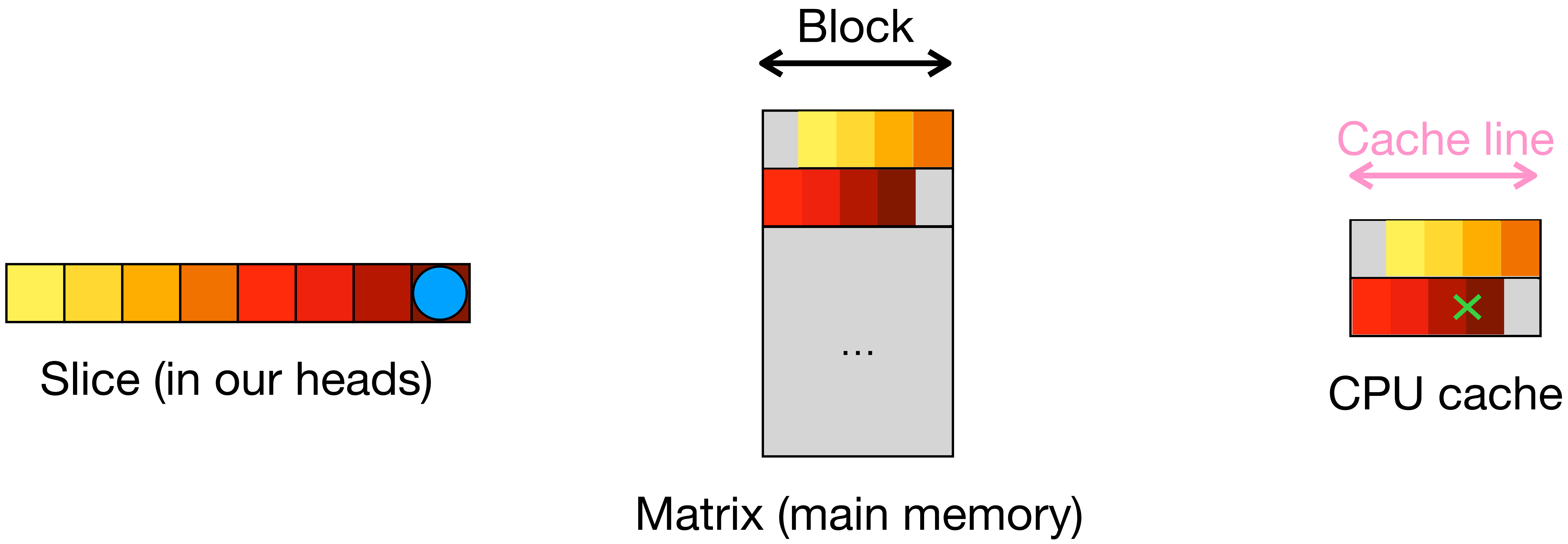

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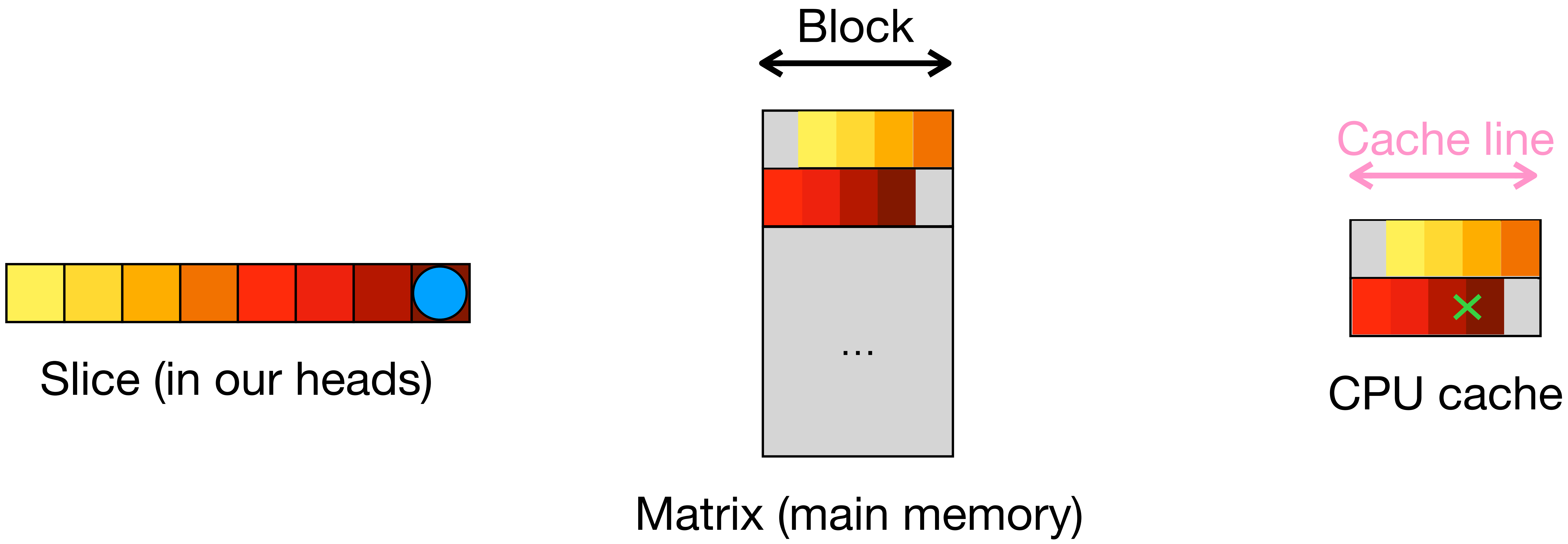

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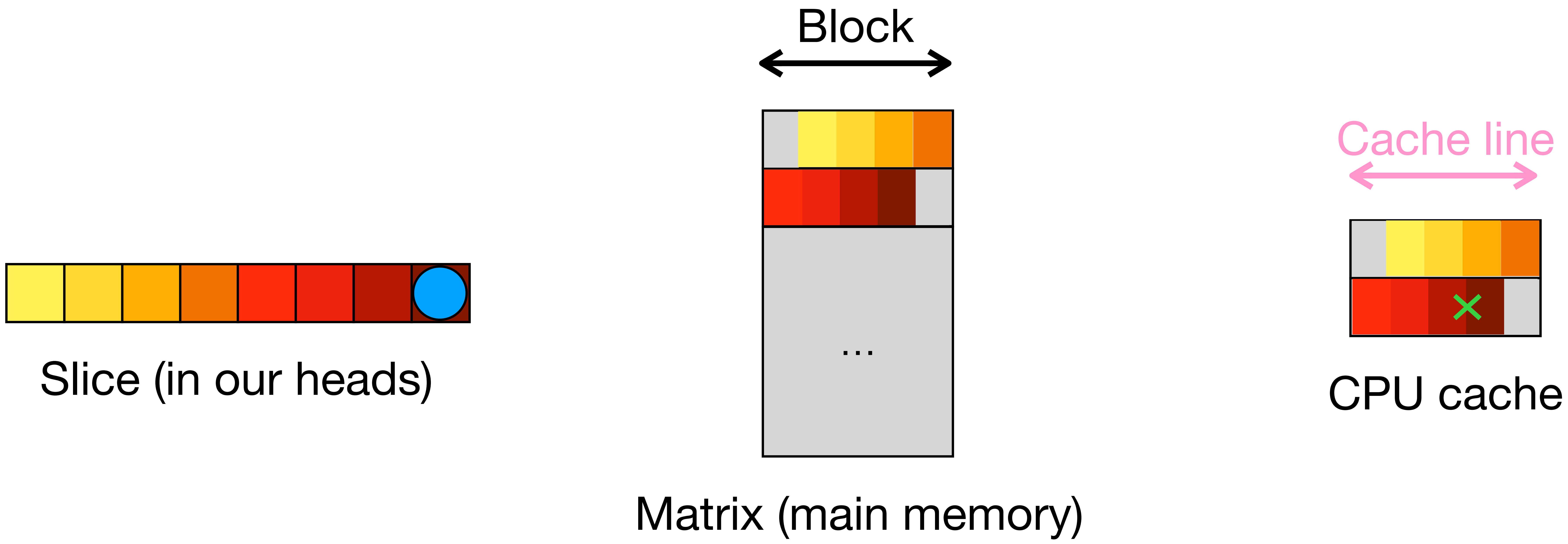

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- Cache placement policy (L1, L2 or L3?)

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- … and **predictability**

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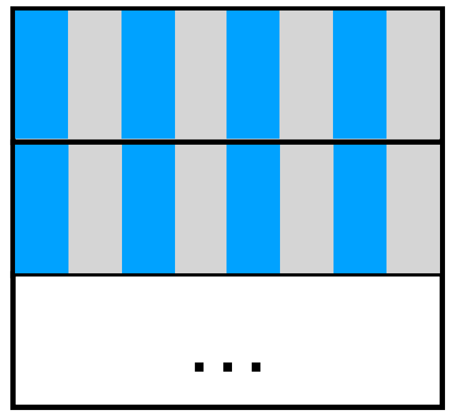

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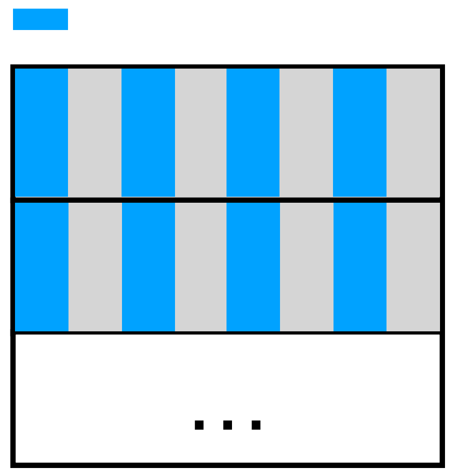

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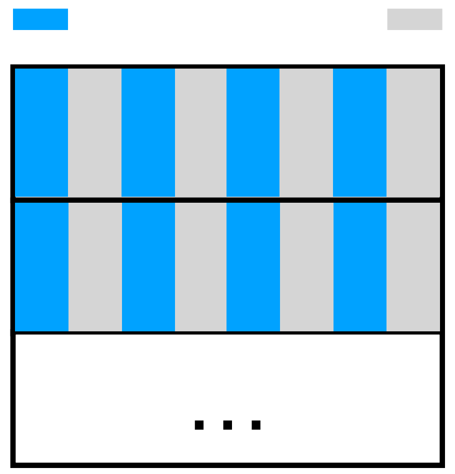

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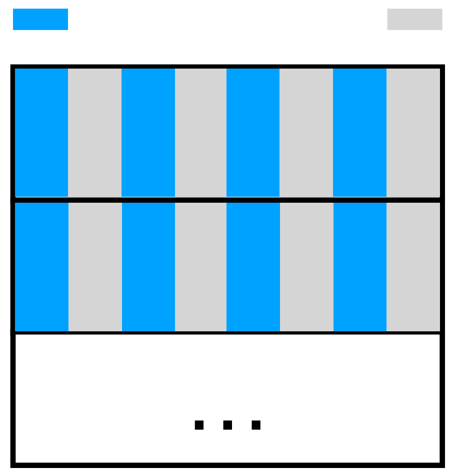

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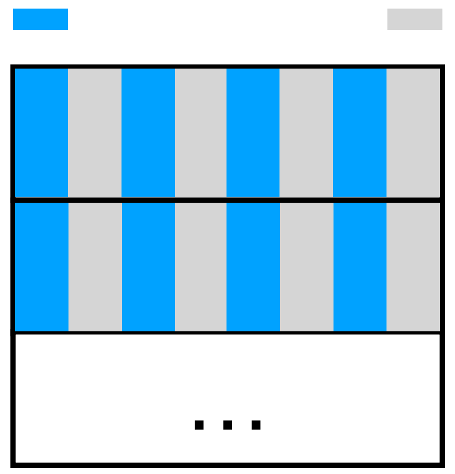

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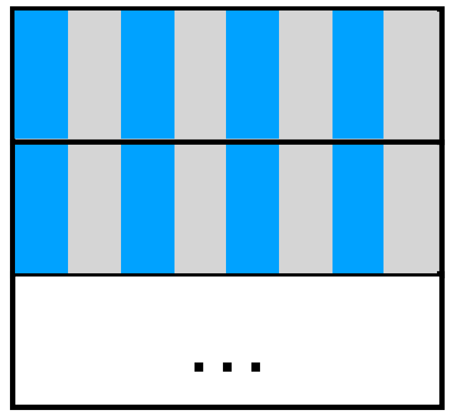

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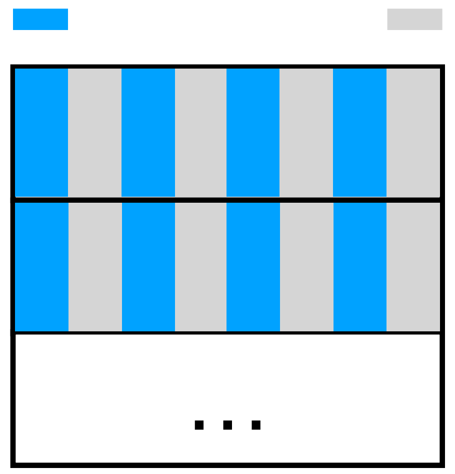

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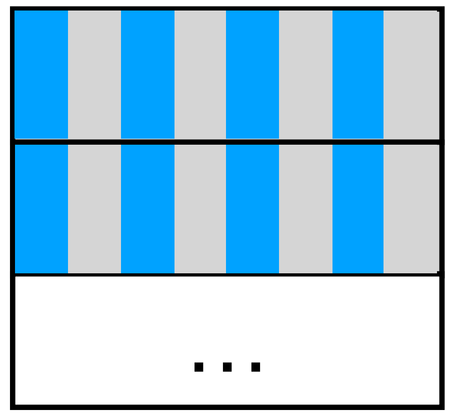

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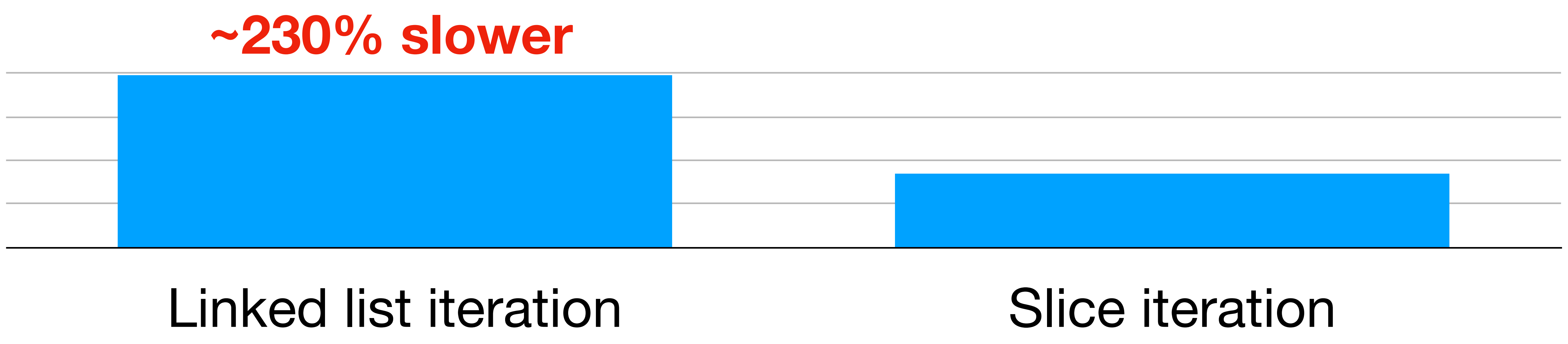

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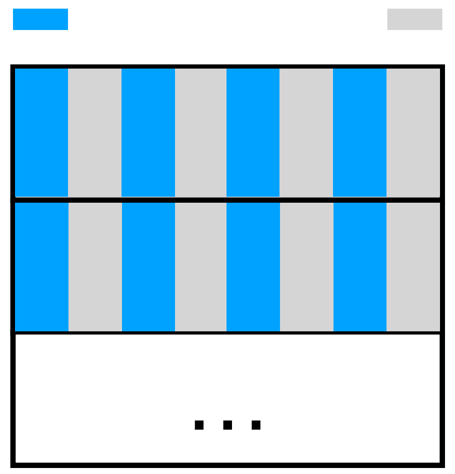

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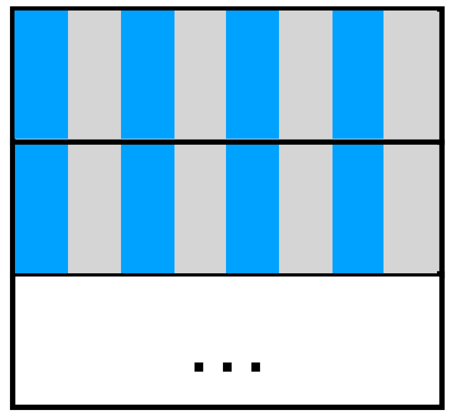

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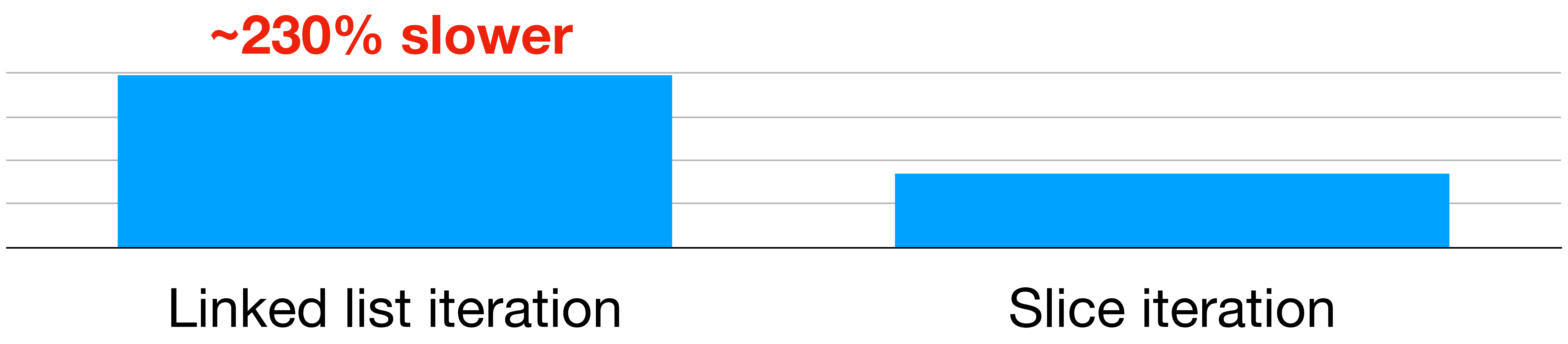

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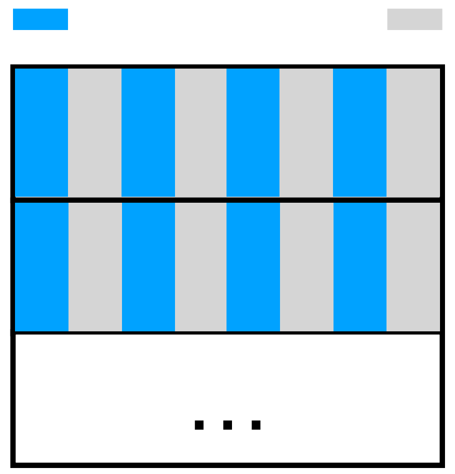

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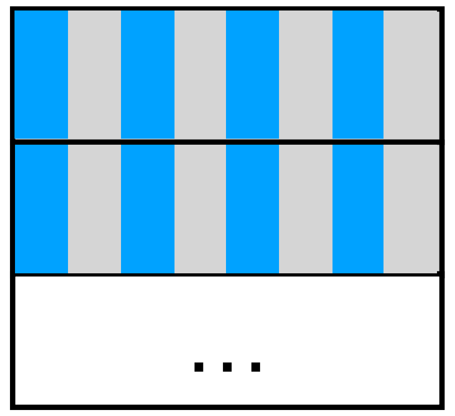

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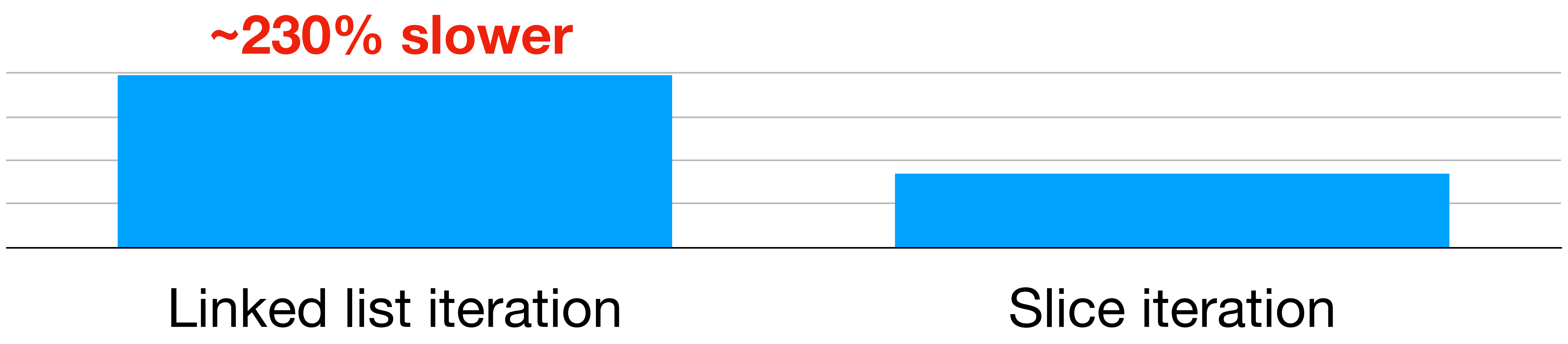

- **Possible** spatial locality
- But **not predictable** for the CPU (no line fetching)

Backwards Iteration

- What if we iterate **backwards** on a slice?

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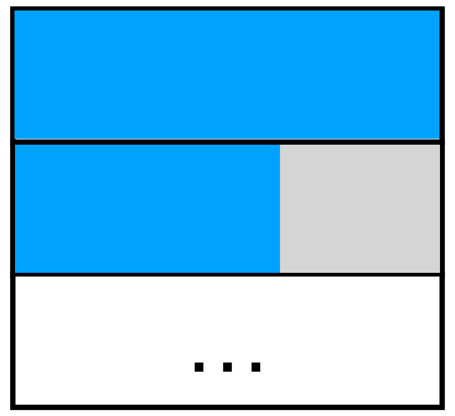

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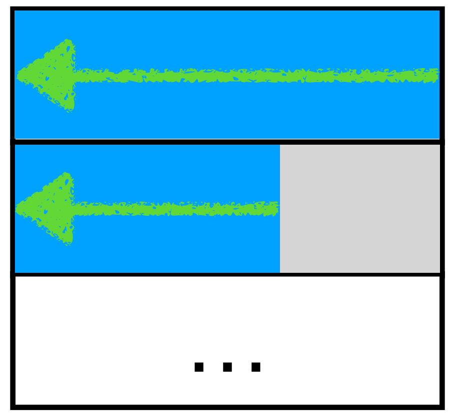

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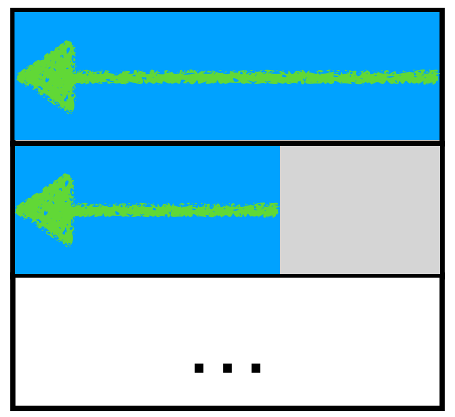

Main memory

Forwards

```go
for i := 0; i < length; i++ {
    r = s[i]
}
```

Backwards

```go
for i := length - 1; i >= 0; i-- {
    r = s[i]
}
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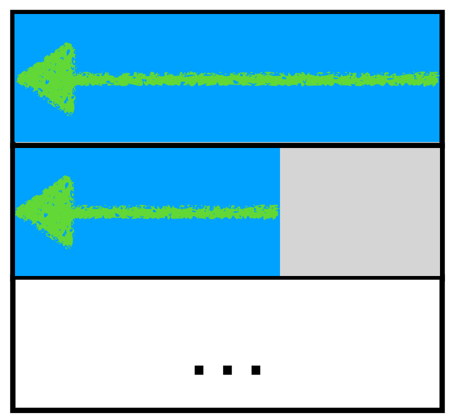

Main memory

Forwards

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for i := 0; i < length; i++ {
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```go
for i := length - 1; i >= 0; i-- {
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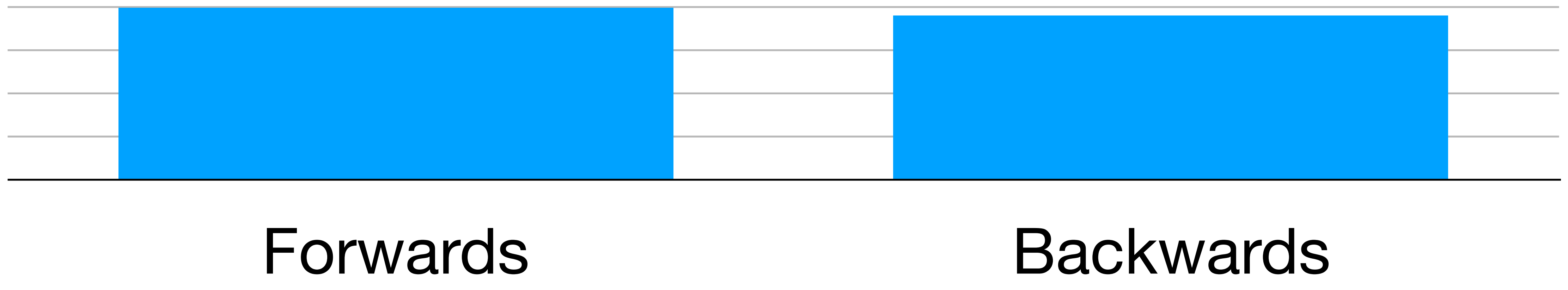

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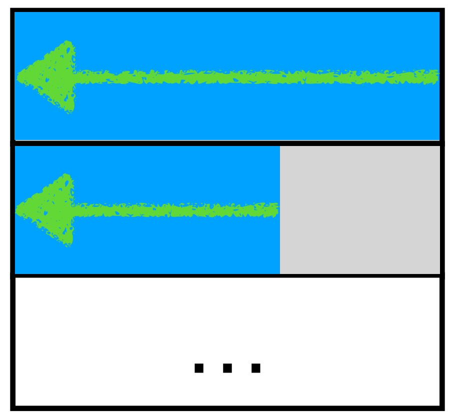

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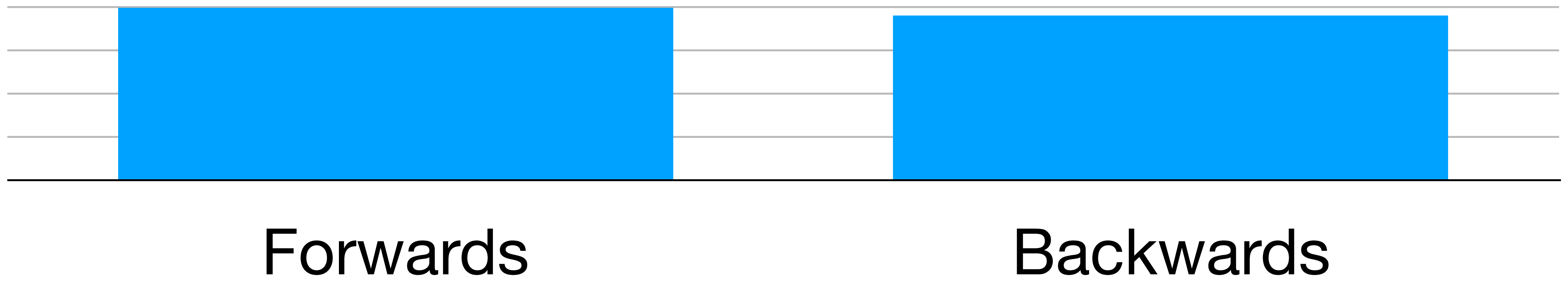

- Spatial locality

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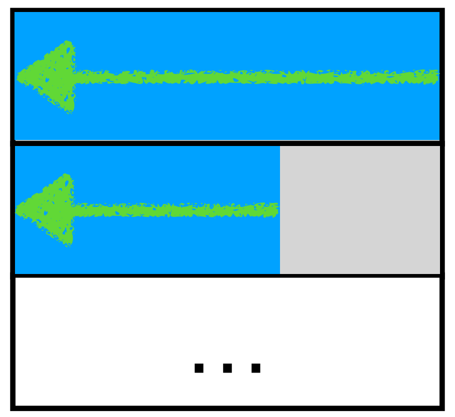

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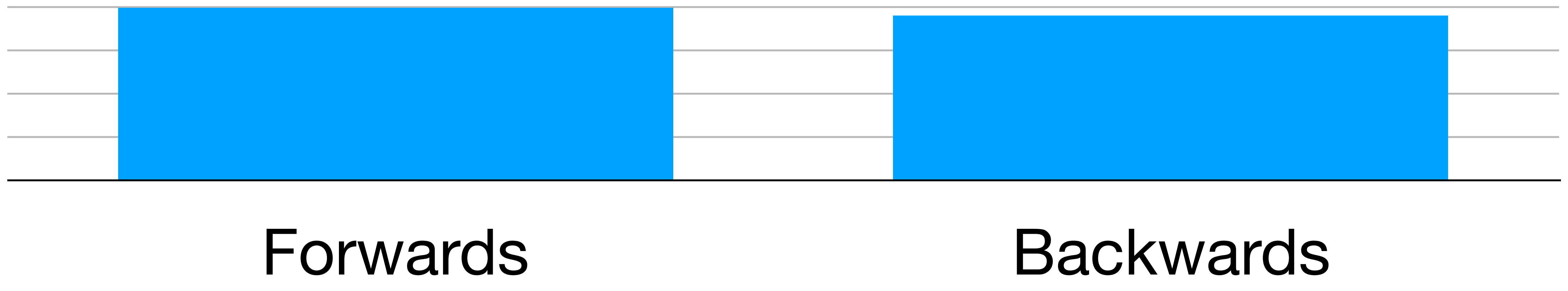

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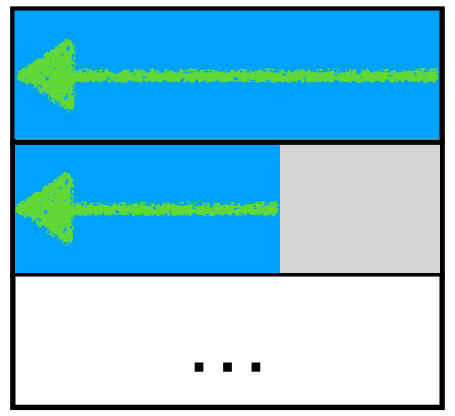

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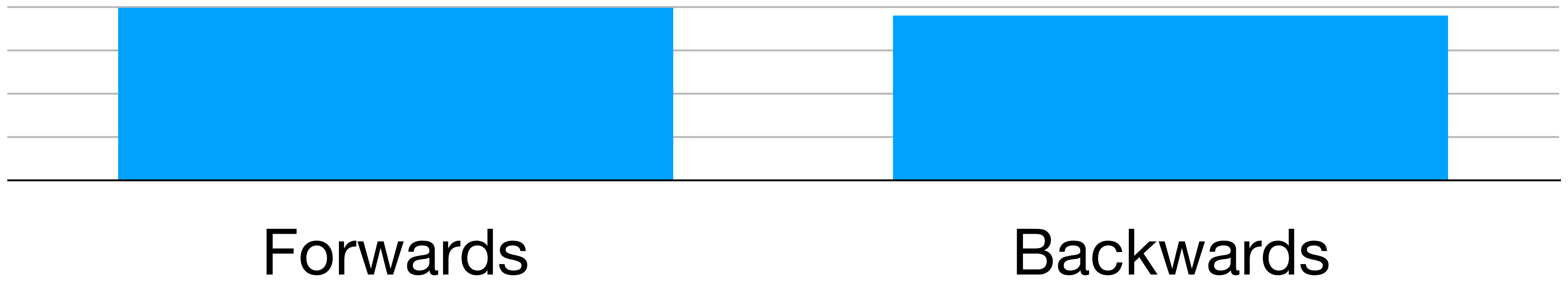

- Spatial locality
- The CPU was able to **predict** that we iterate backwards
- Slightly faster because the bound check is faster

How to Make Things Predictable?

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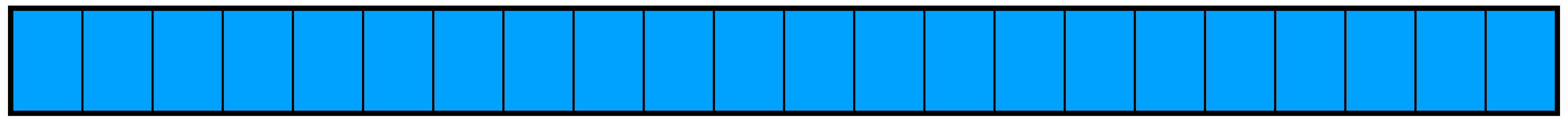

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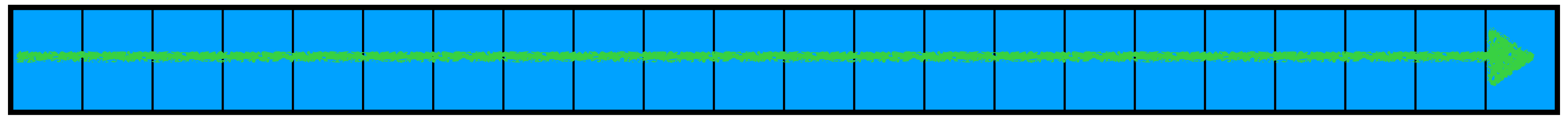

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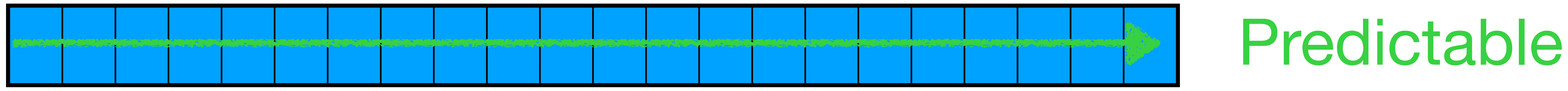

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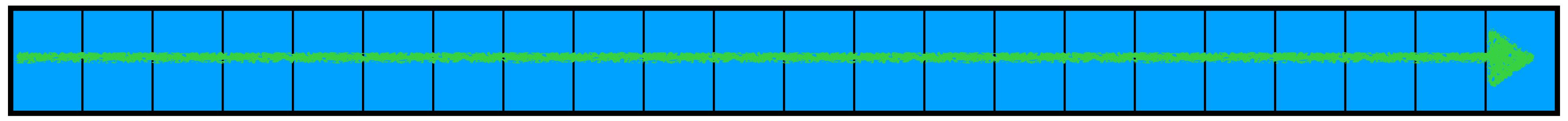

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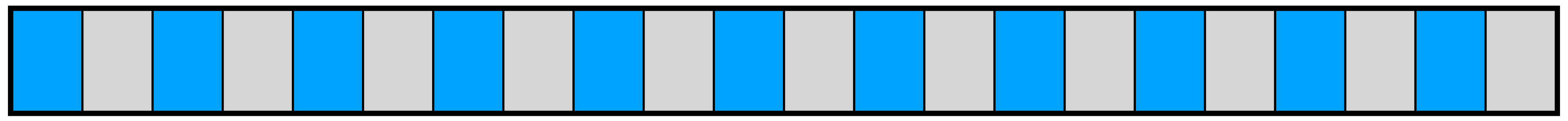

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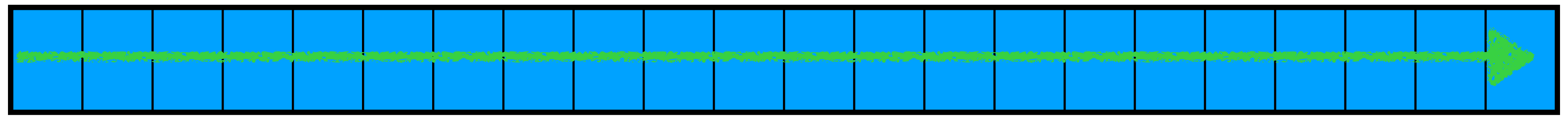

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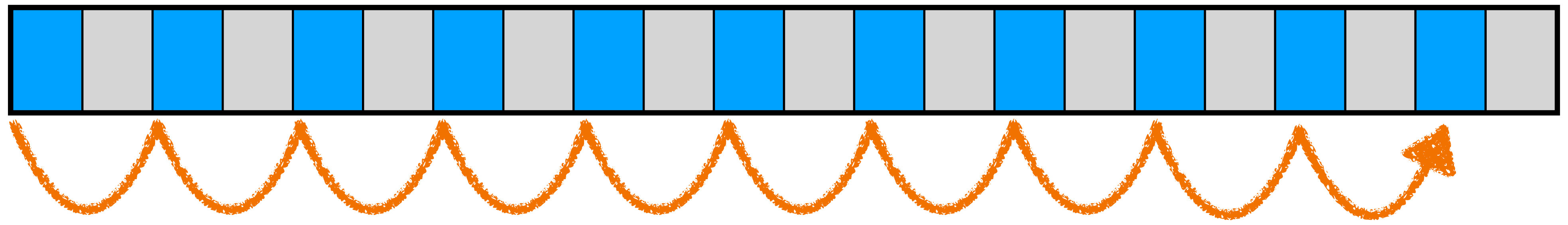

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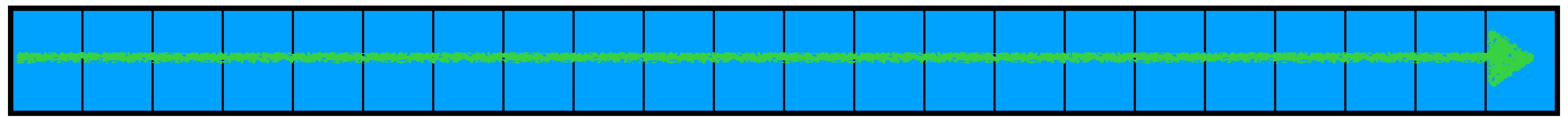

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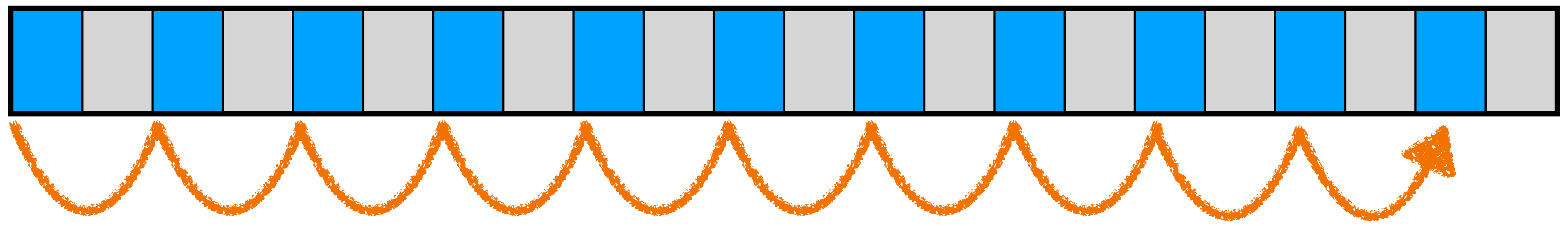

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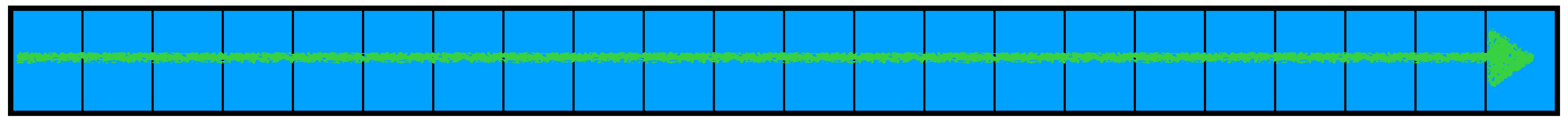

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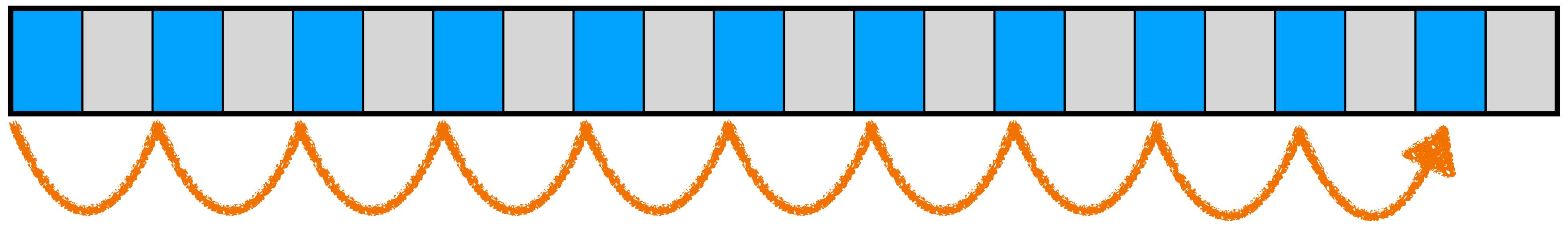

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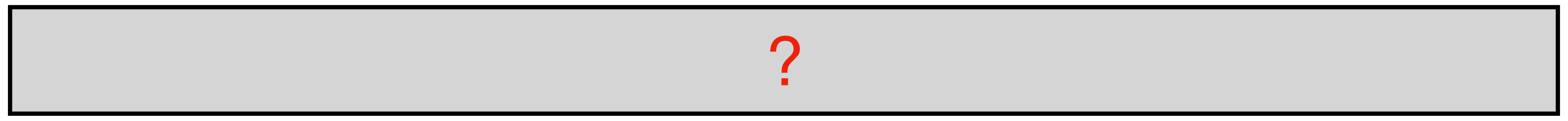

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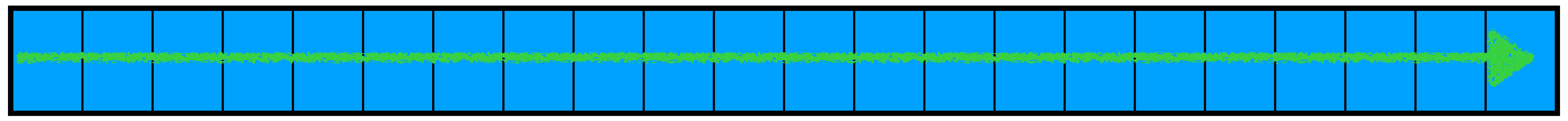

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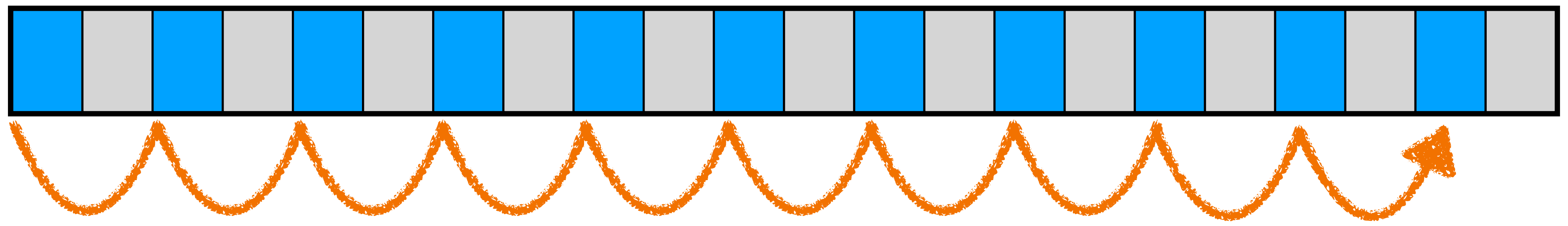

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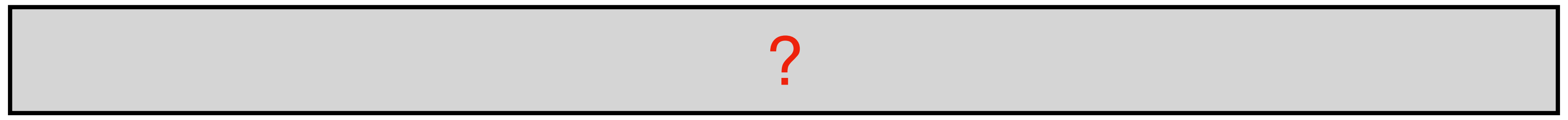

Not predictable

GOPHERCON
TURKEY

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- I can **help** the CPU if my application leverages:
    - **Locality of reference**
    - **Predictability**

CPU Architecture

Locality of Reference

Data-Oriented Design

Caching Pitfall

Concurrency

Data-Oriented Design

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- "The purpose of all programs and all parts of those programs is to **transform data** from one form to another" - Mike Acton

- Object-Oriented design is a way to mirror how we interact with the real world

- Yet, hardware does not like objects

- Data-Oriented design is about organising data in a way to get the **most value out of each cache line**

Data-Oriented Design

- 2 concrete examples:
  - Structure alignment
  - Slice of structures vs structure of slices

Structure Alignment

Structure Alignment

```go
type I1 struct {
    b1 bool
    i  int64
    b2 bool
}

func BenchmarkI1(b *testing.B) {
    s := make([]I1, it)
    var r int64
    b.ResetTimer()
    for j := 0; j < it; j++ {
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}
```

```go
type I2 struct {
    i  int64
    b1 bool
    b2 bool
}

func BenchmarkI2(b *testing.B) {
    s := make([]I2, it)
    var r int64
    b.ResetTimer()
    for j := 0; j < it; j++ {
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    }
    result = r
}
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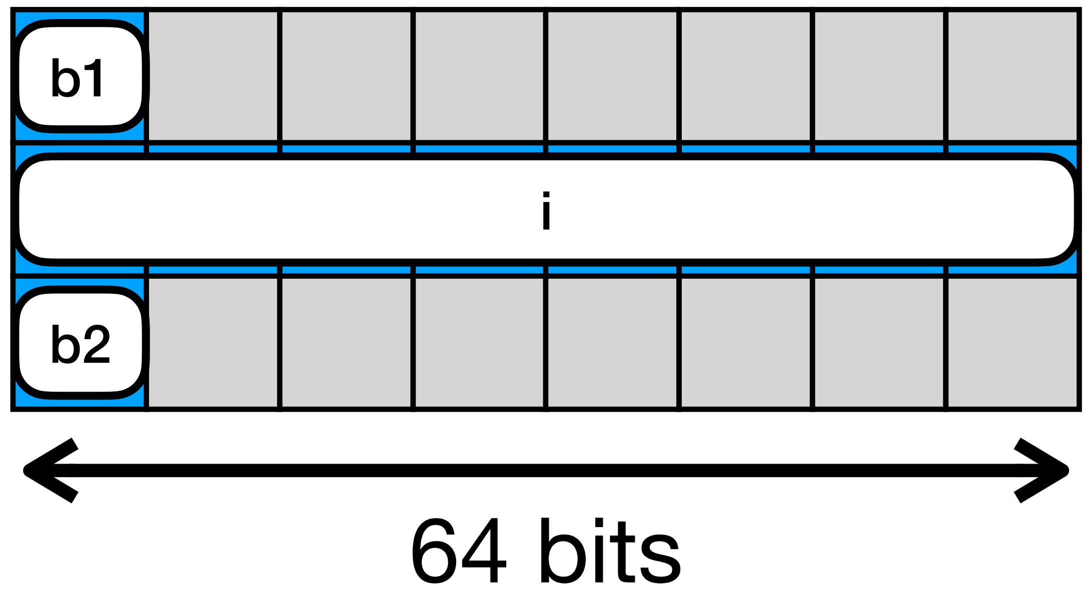

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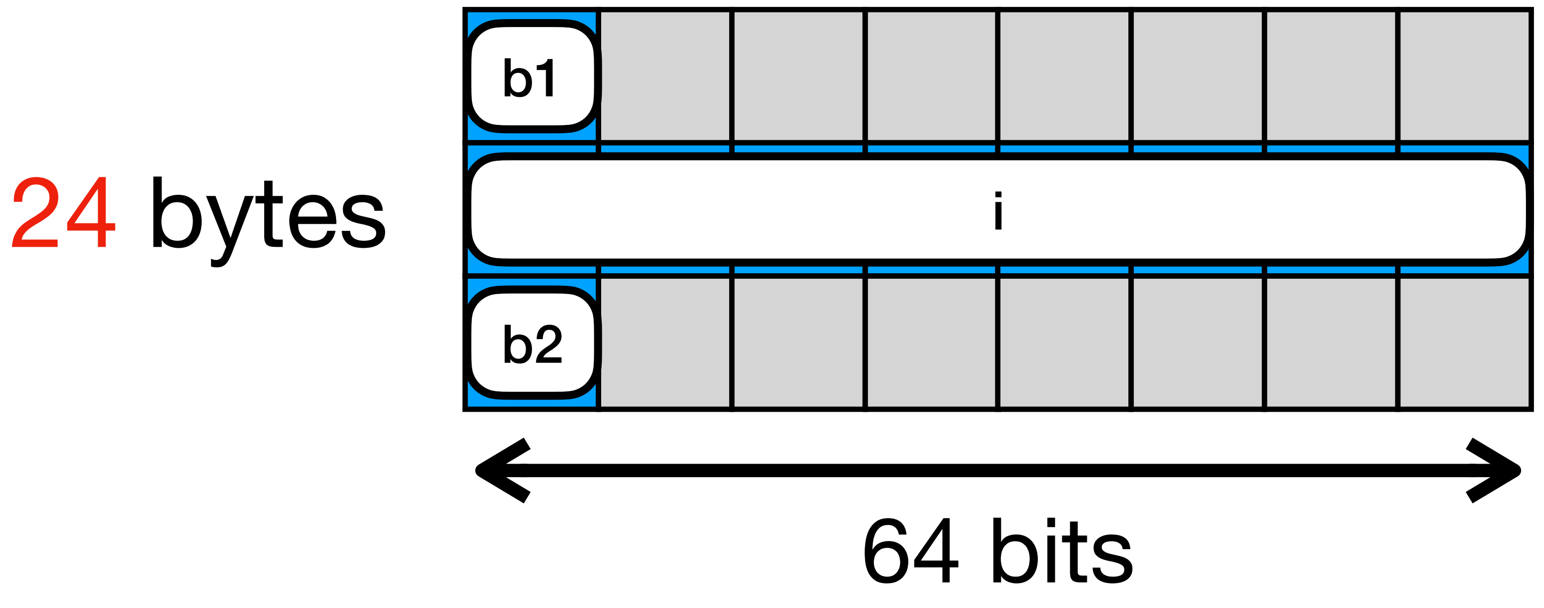

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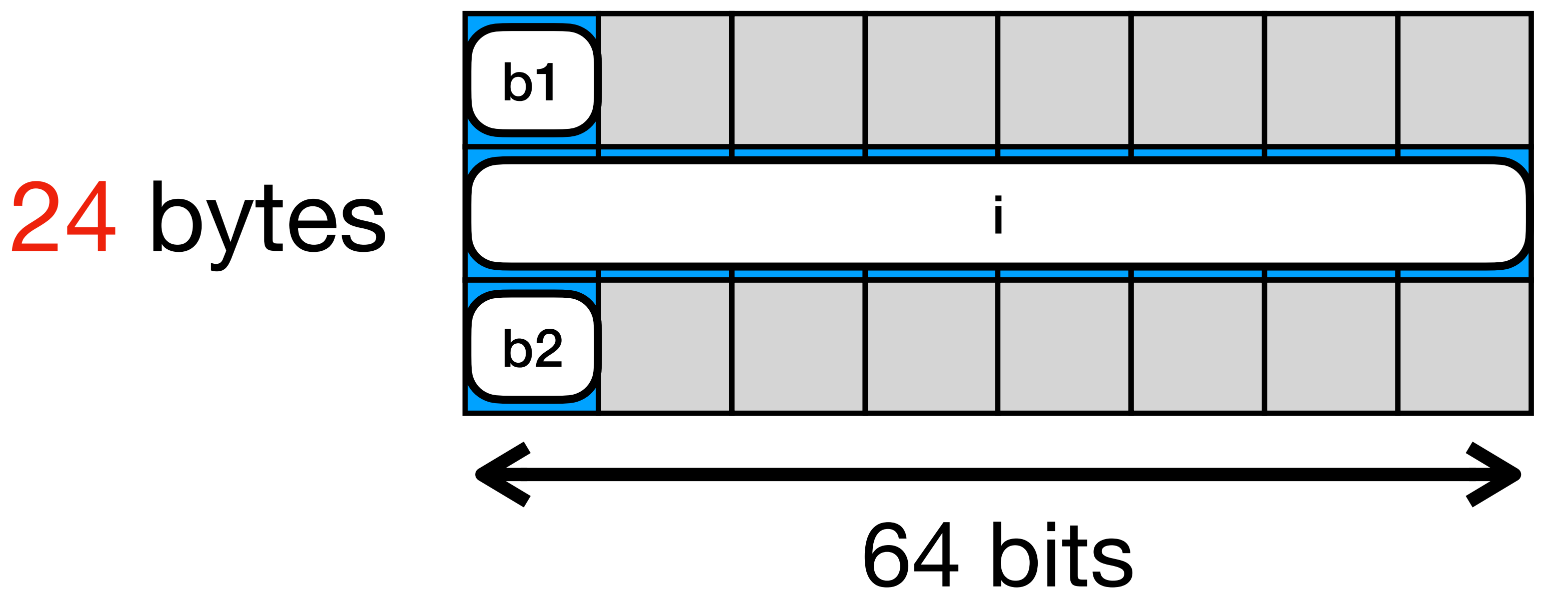

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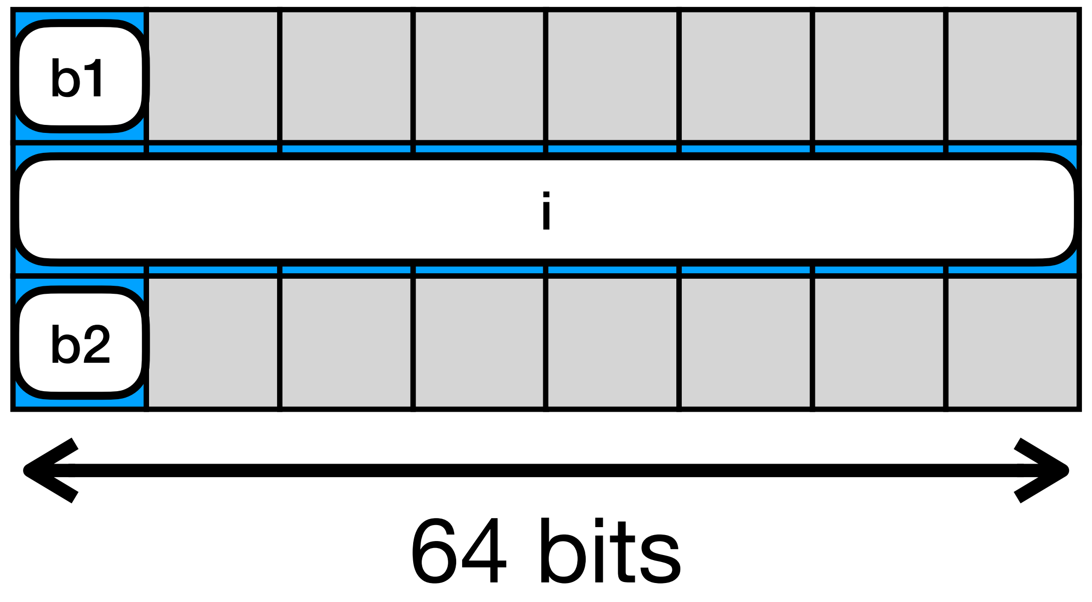
24 bytes



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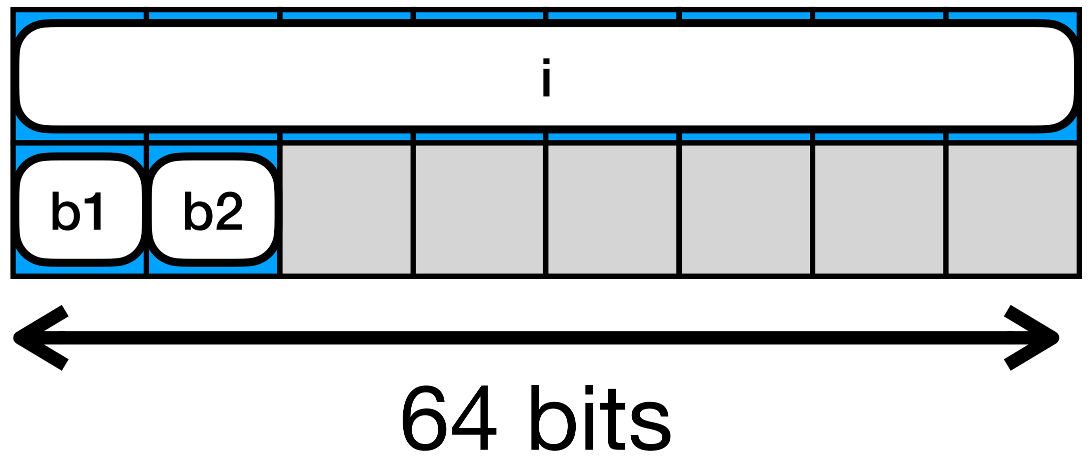

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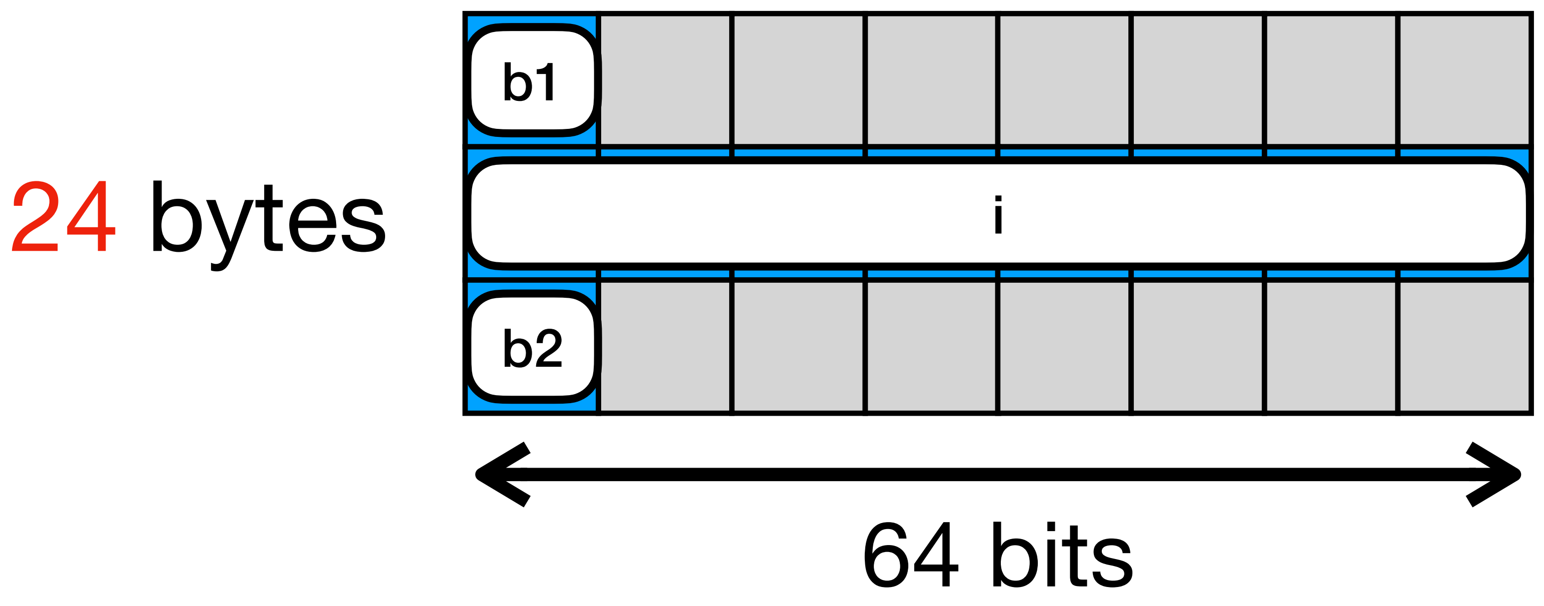

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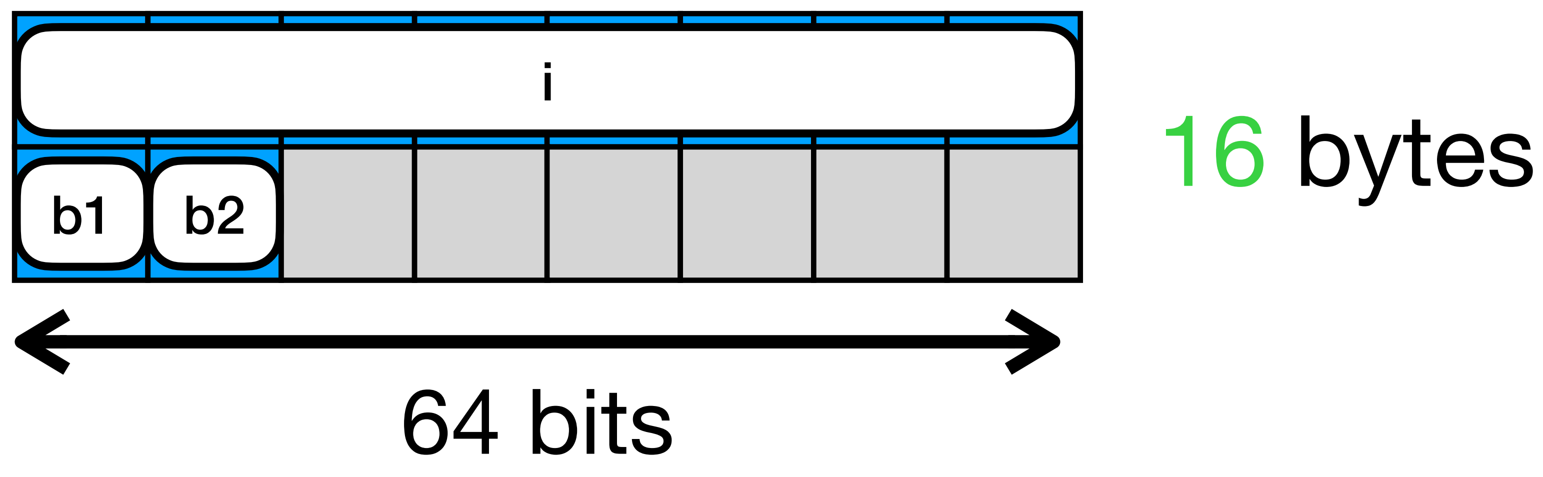

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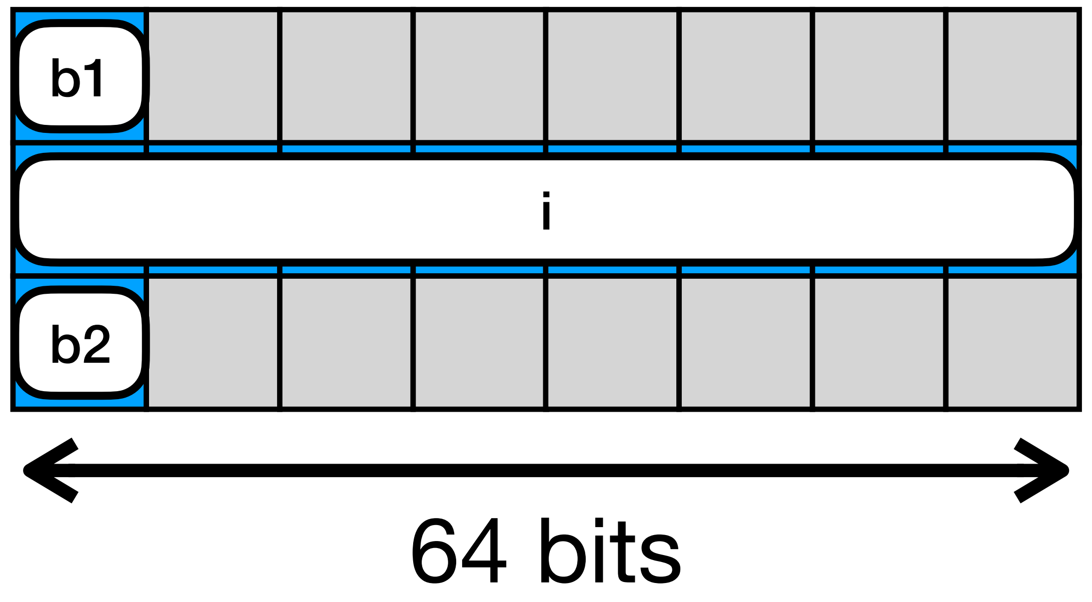

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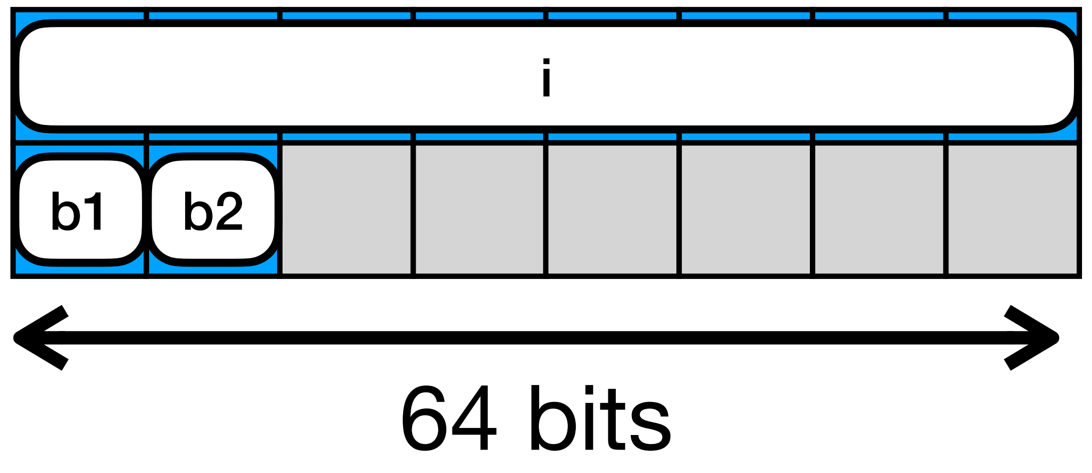

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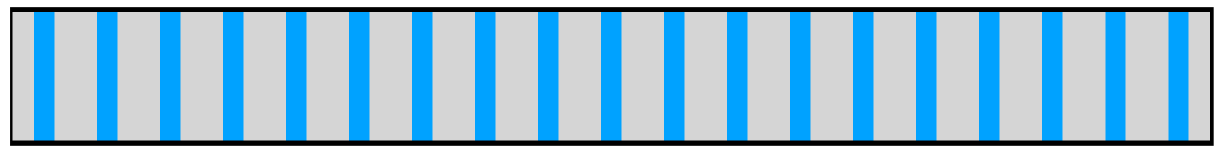

In memory

10k slice: 3750 cache lines
(cache line: 64 bytes)

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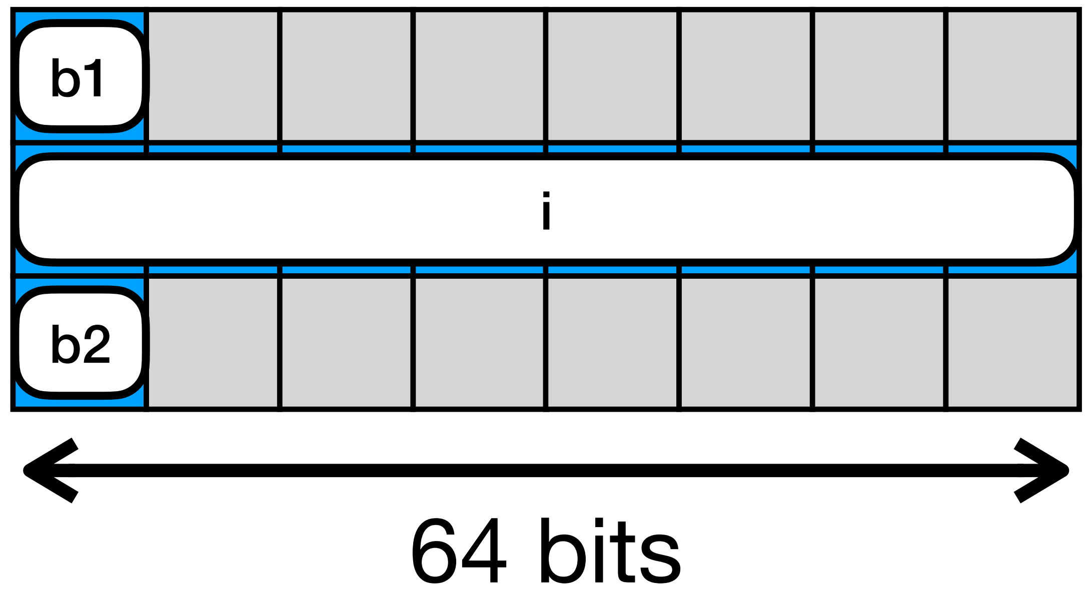

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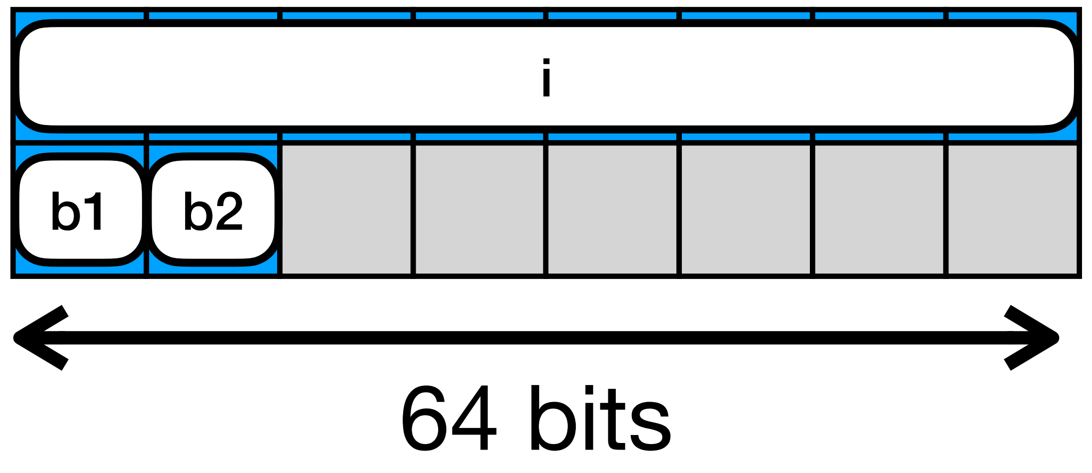

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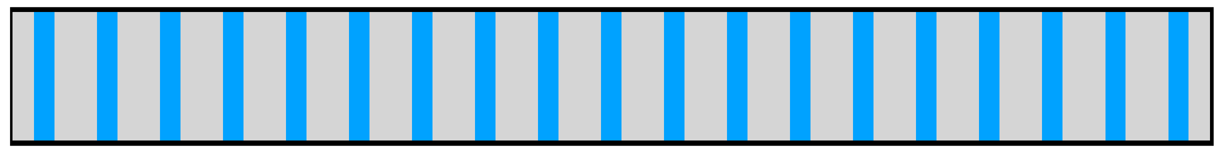

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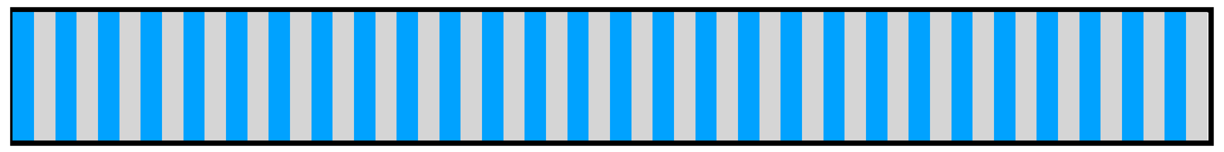

10k slice: 3750 cache lines
(cache line: 64 bytes)

10k slice: 2500 cache lines

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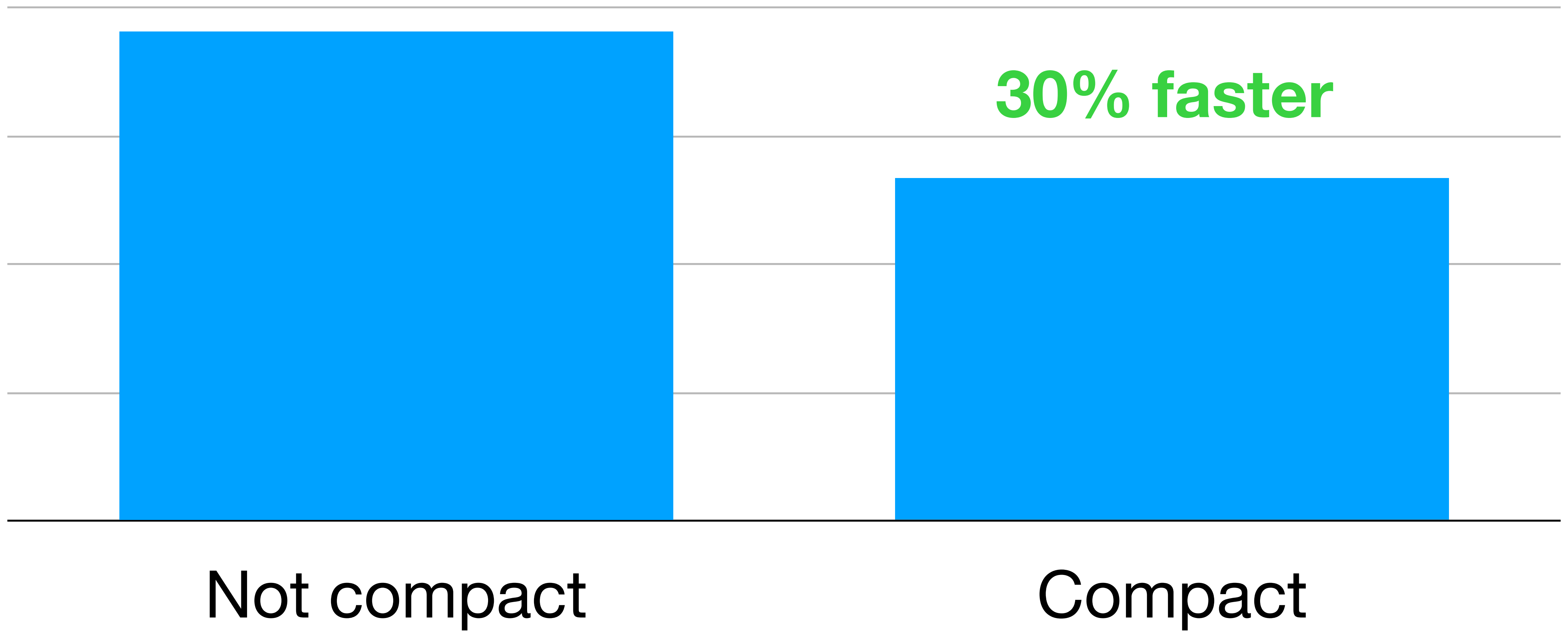

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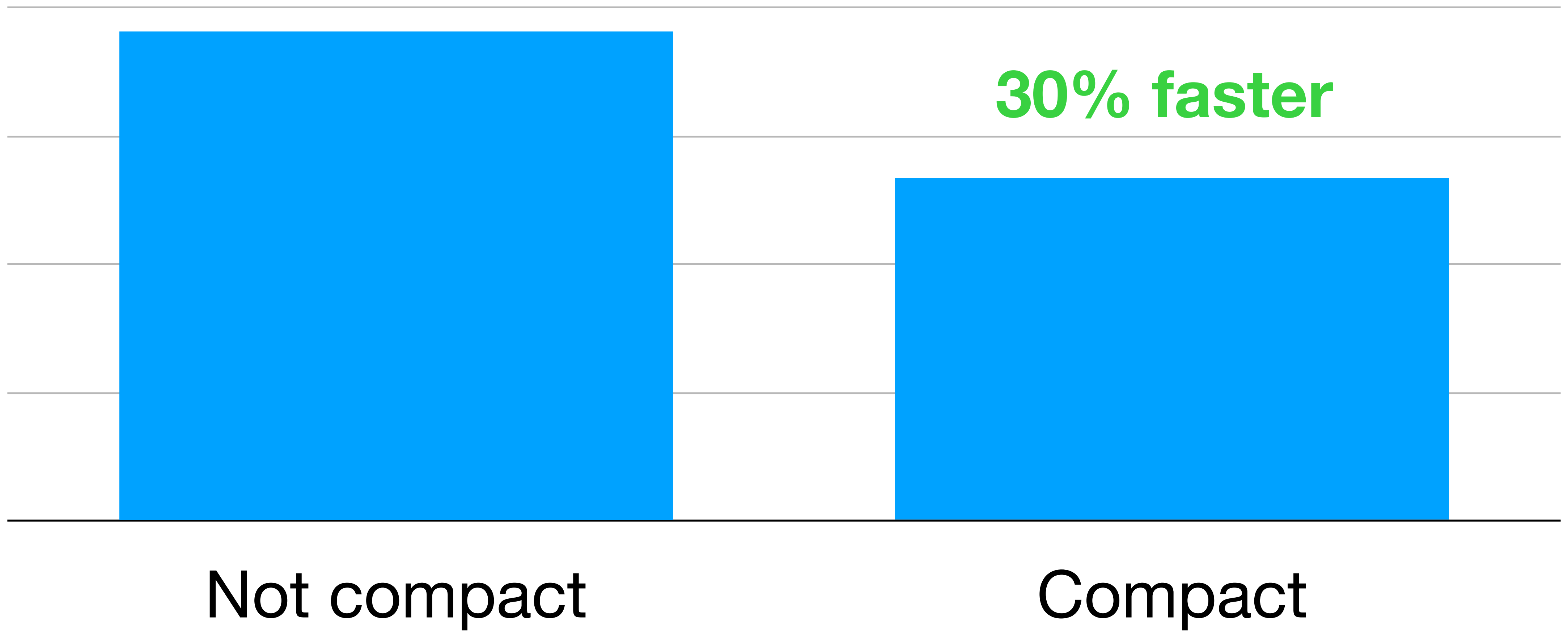

- Memory footprint (GC pressure)

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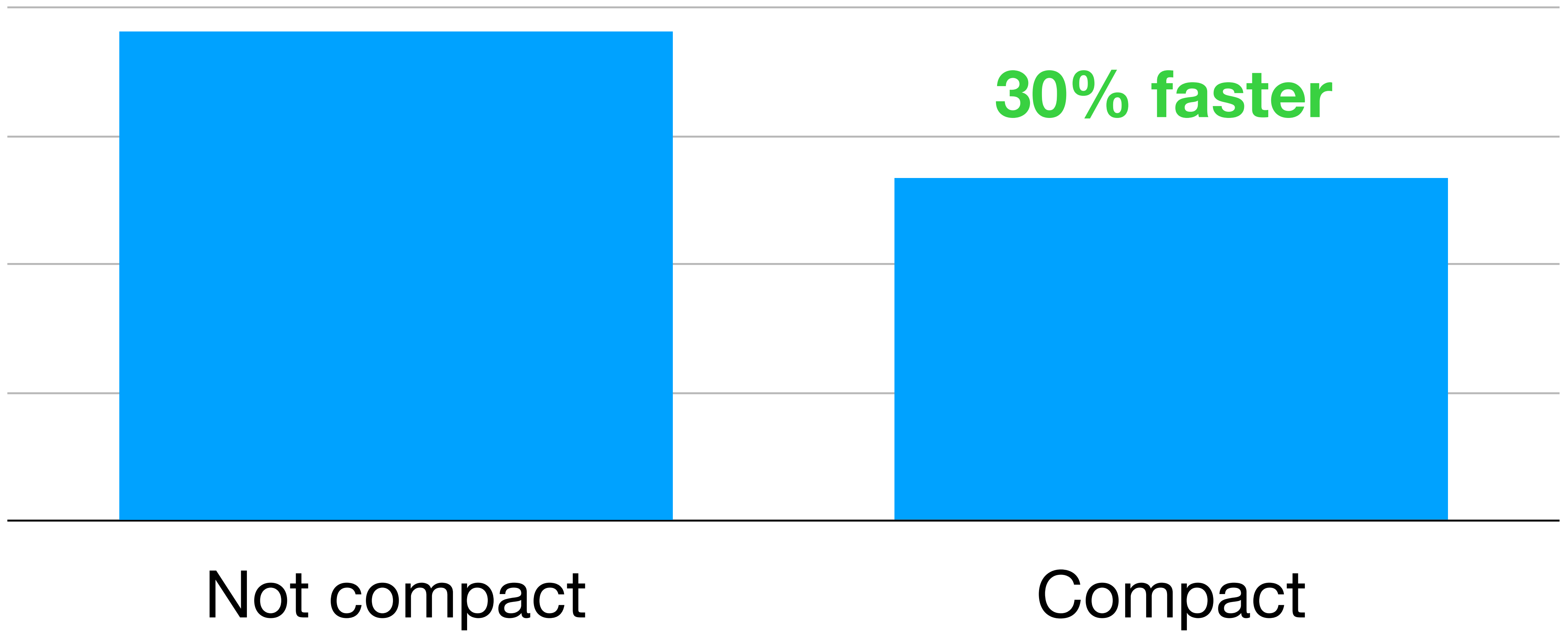

- Memory footprint (GC pressure)
- Iterating over a **compact** data structure is more efficient as it requires **less caches lines**

Slice of Structures vs Structure of Slices

Slice of Structures vs Structure of Slices

```go
type Struct1 struct {
    a int32
    b int64
}

func BenchmarkSliceOfStructures(b *testing.B) {
    s := make([]Struct1, it)
    var r int32
    b.ResetTimer()
    for i := 0; i < b.N; i++ {
        for i := 0; i < it; i++ {
            r = s[i].a
        }
    }
    result = r
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		}
	}
	result = r
}
```

```go
type Struct2 struct {
	a []int32
	b []int64
}

func BenchmarkStructureOfSlices(b *testing.B) {
	s := Struct2{
		a: make([]int32, it),
		b: make([]int64, it),
	}
	var r int32
	b.ResetTimer()
	for i := 0; i < b.N; i++ {
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			r = s.a[i]
		}
	}
	result = r
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```

Slice of Structures vs Structure of Slices

```go
type Struct1 struct {
    a int32
    b int64
}

func BenchmarkSliceOfStructures(b *testing.B) {
    s := make([]Struct1, it)
    var r int32
    b.ResetTimer()
    for i := 0; i < b.N; i++ {
        for i := 0; i < it; i++ {
            r = s[i].a
        }
    }
    result = r
}
```

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type Struct2 struct {
    a []int32
    b []int64
}

func BenchmarkStructureOfSlices(b *testing.B) {
    s := Struct2{
        a: make([]int32, it),
        b: make([]int64, it),
    }
    var r int32
    b.ResetTimer()
    for i := 0; i < b.N; i++ {
        for i := 0; i < it; i++ {
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GOPHERCON TURKEY

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Struct of slices

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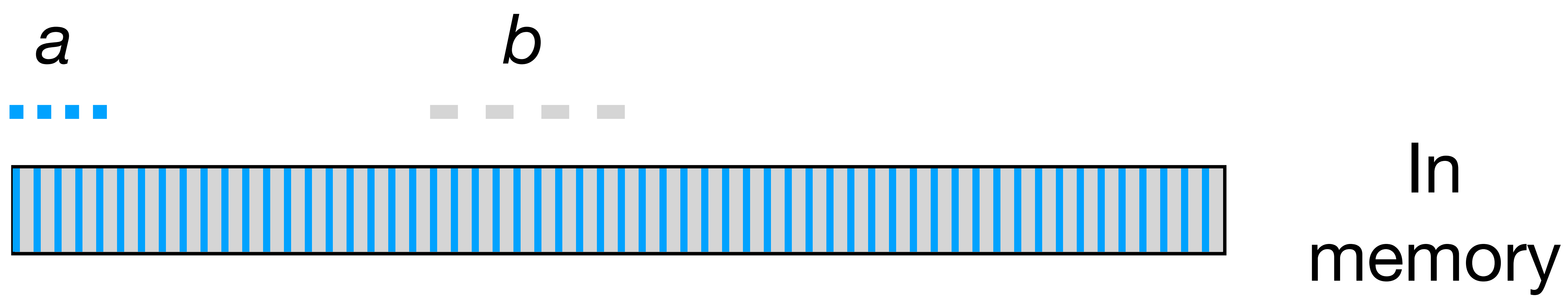

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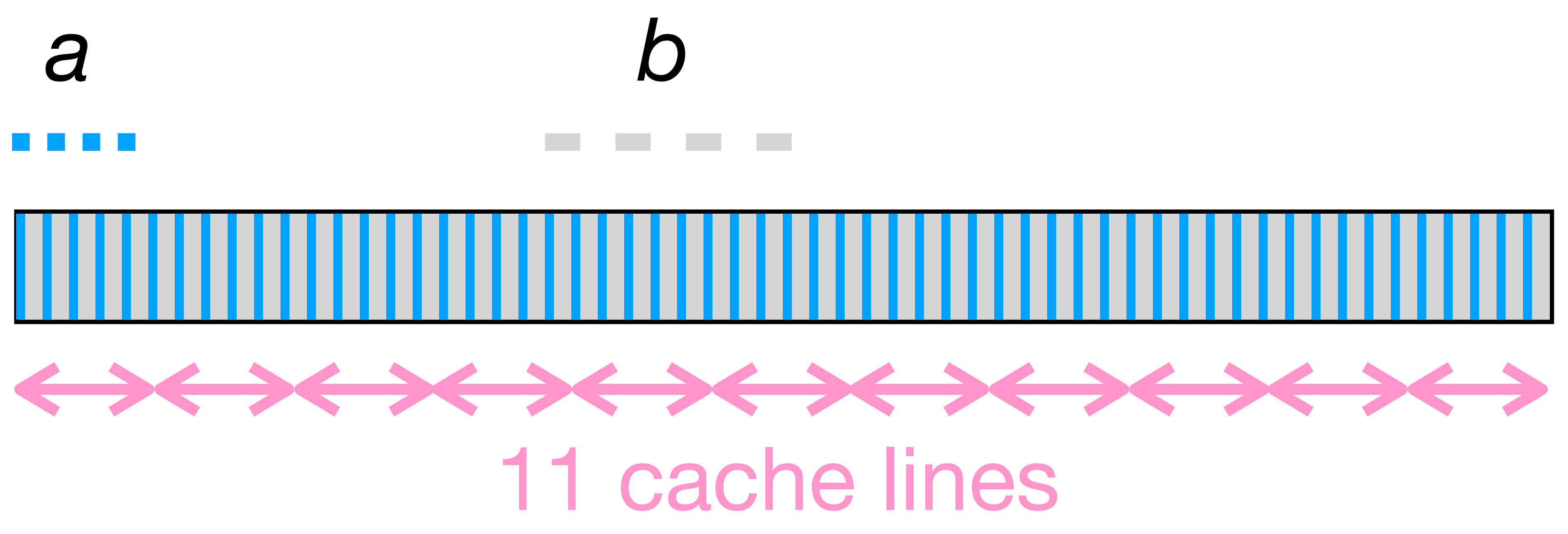

In memory

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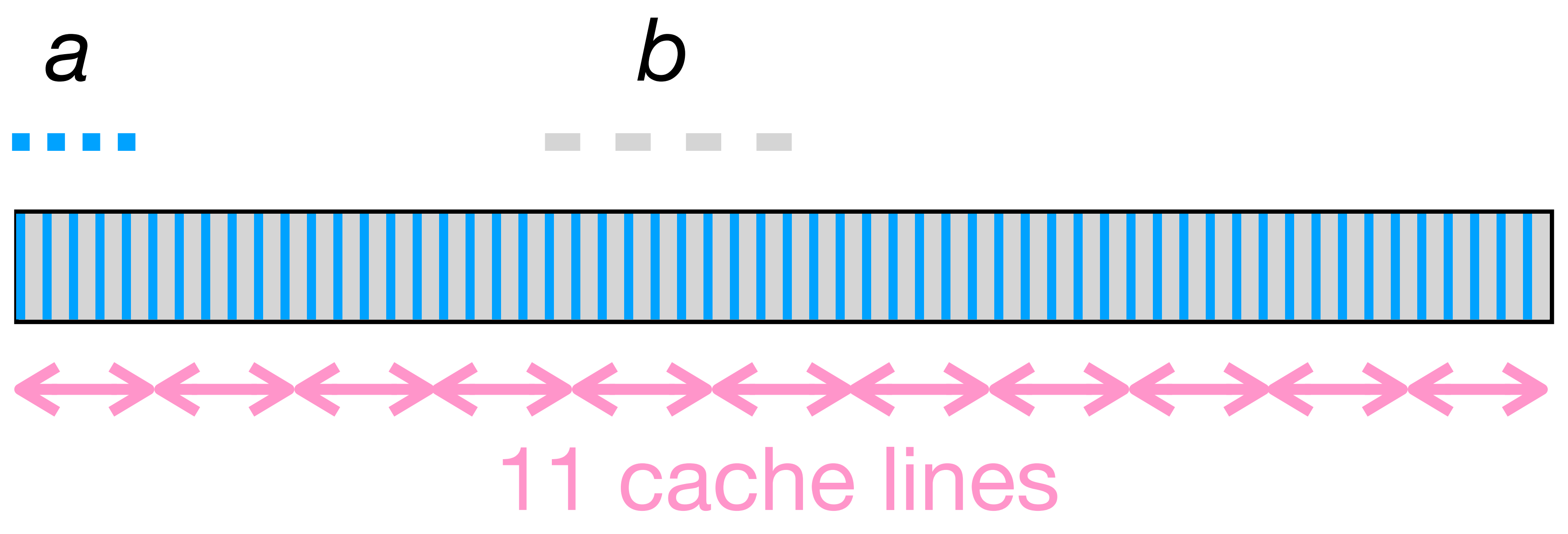

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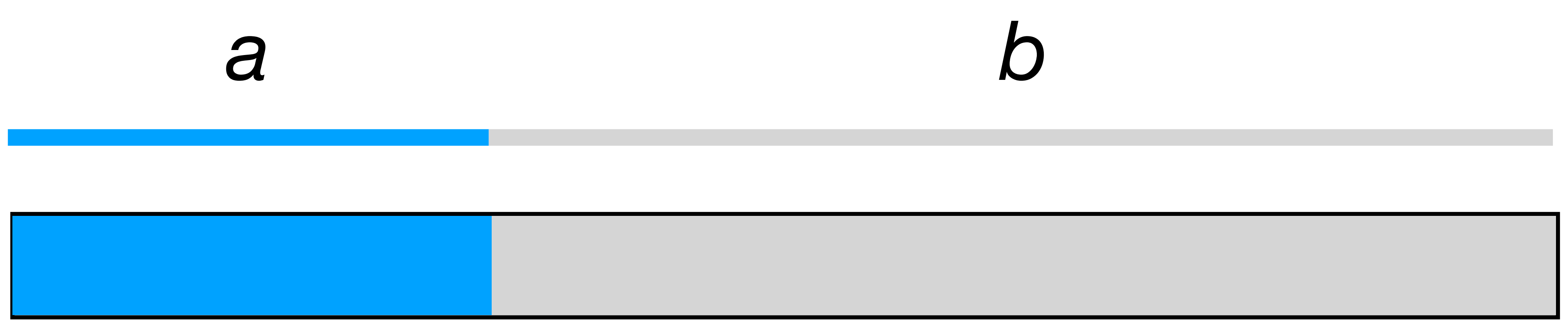

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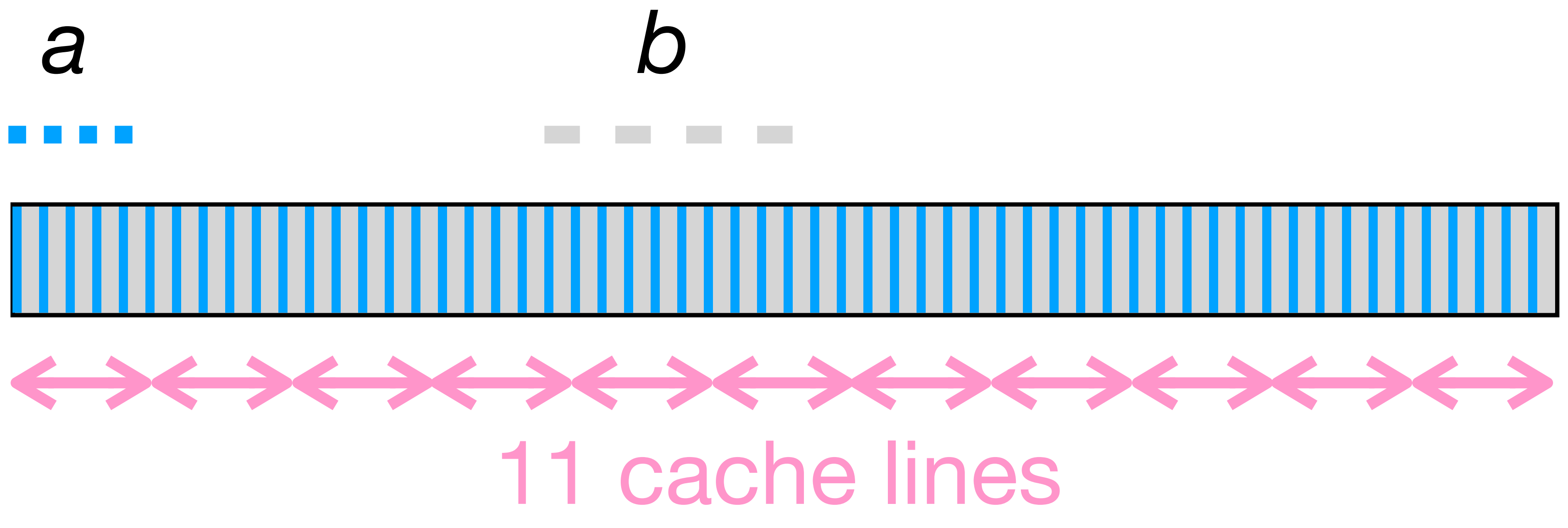

In memory

Constant stride

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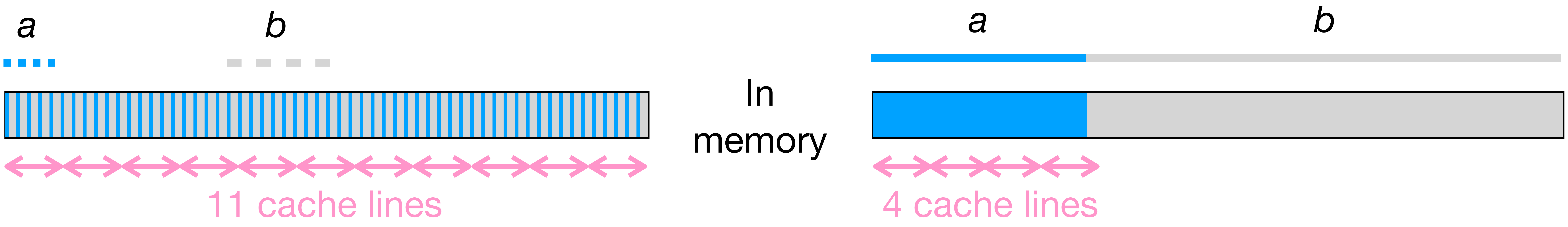

GOPHERCON TURKEY

Slice of structs

Constant stride

```go
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    a int32
    b int64
}
s := make([]Struct1, it)
```
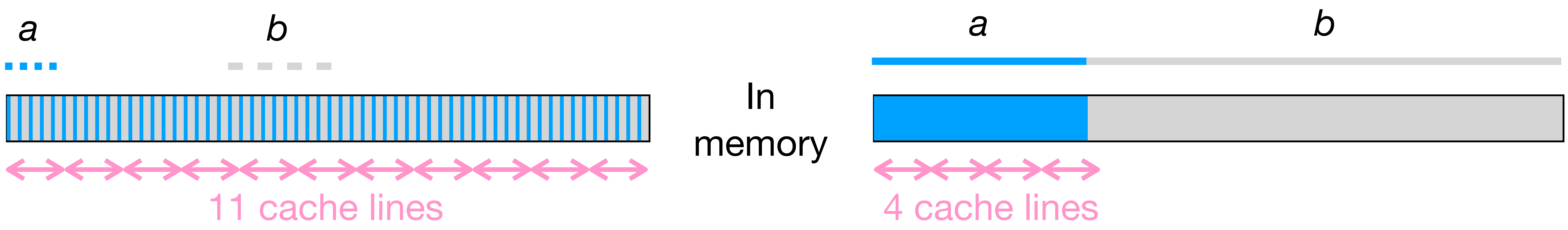

Struct of slices

Unit stride

```go
type Struct2 struct {
    a []int32
    b []int64
}
s := Struct2{
    a: make([]int32, it),
    b: make([]int64, it),
}
```



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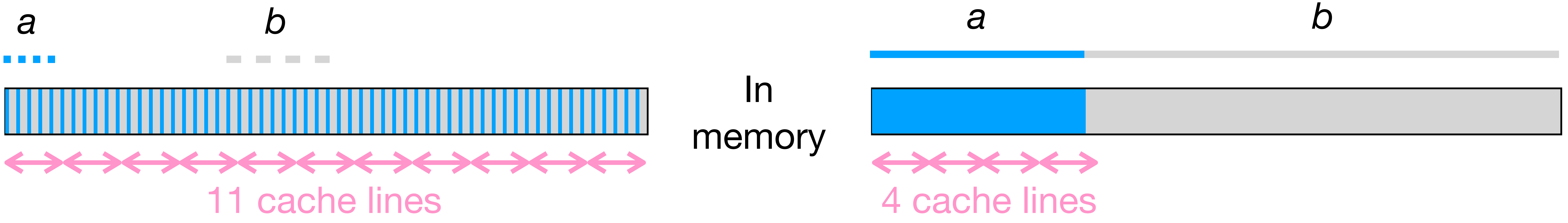

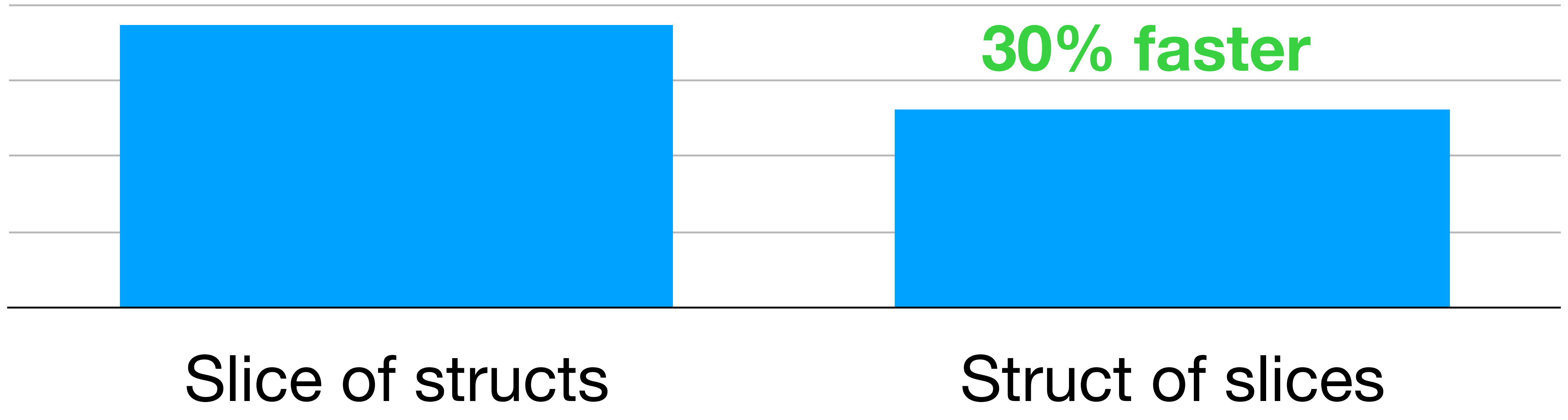

Slice of Structures vs Structure of Slices

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- A concrete example: Go standard **flate package**

Slice of Structures vs Structure of Slices

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- Flate is a **compression** algorithm based on two other algorithms: huffman encoding an LZ77 compression

Slice of Structures vs Structure of Slices

Go flate package

```go
type hcode struct {
    code, len uint16
}

type huffmanEncoder struct {
    codes     []hcode
    freqcache []literalNode
    bitCount  [17]int32
    lns       byLiteral // stored to avoid repeated allocation in generate
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- Example:

```
for i := 0; i < numCodegens; i++ {
    value := uint(w.codegenEncoding.codes[codegenOrder[i]].len)
    w.writeBits(int32(value), nb: 3)
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- Metrics?

Xcode Instruments

Xcode Instruments

Xcode Instruments

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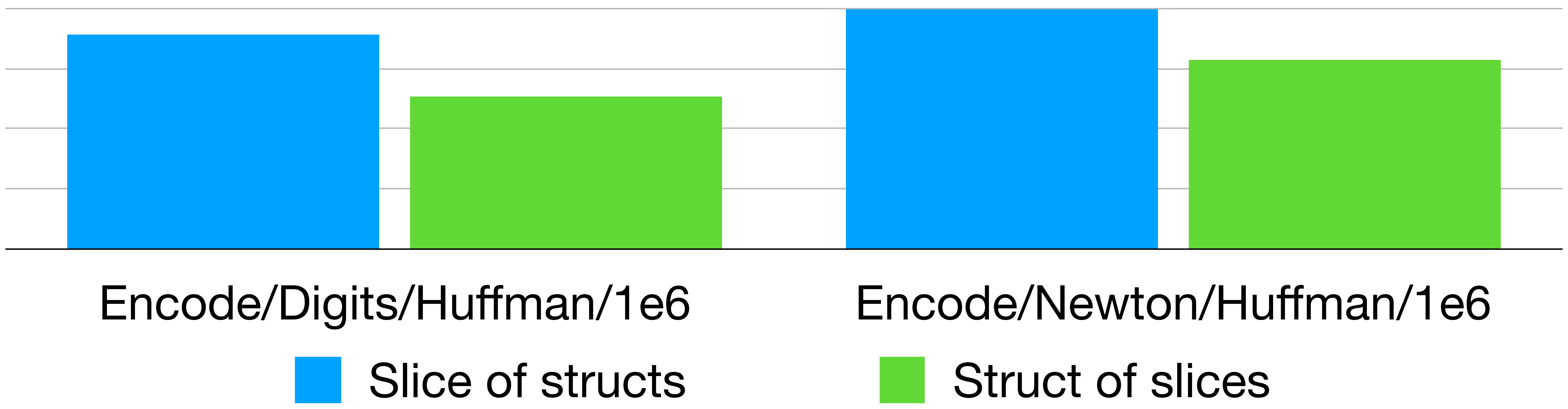

Between **21% and 28% faster**

- I can **design algorithms** to leverage CPU caches

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- I can also **organise my data** to get the most value out of cache lines

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- **Unit stride** > Constant stride > Non-unit stride

CPU Architecture

Locality of Reference

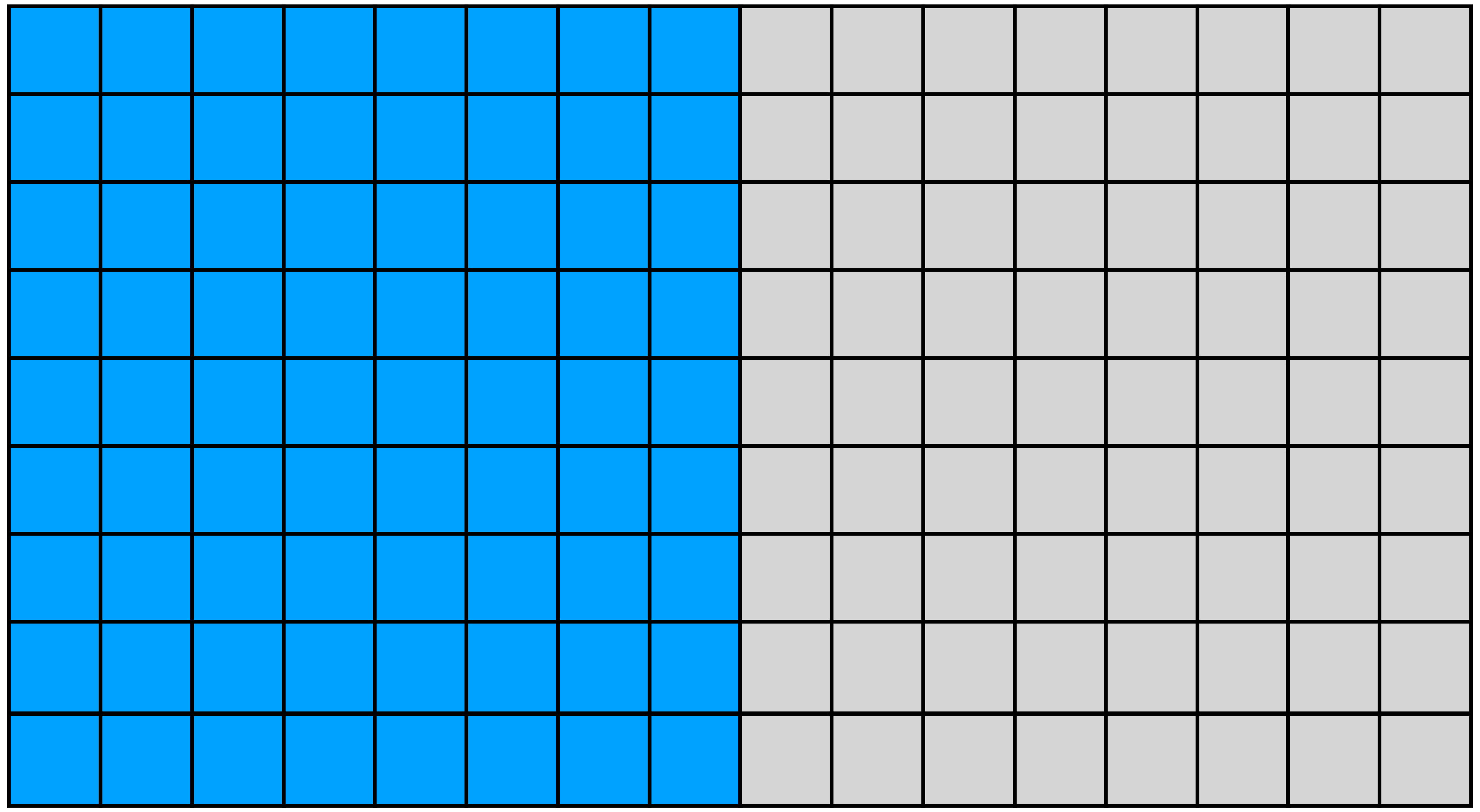
Data-Oriented Design

Caching Pitfall

Concurrency

GOPHERCON
TURKEY

- Two-dimensional array of int64s
  64 bytes cache line (8 elements)



- Two-dimensional array of int64s
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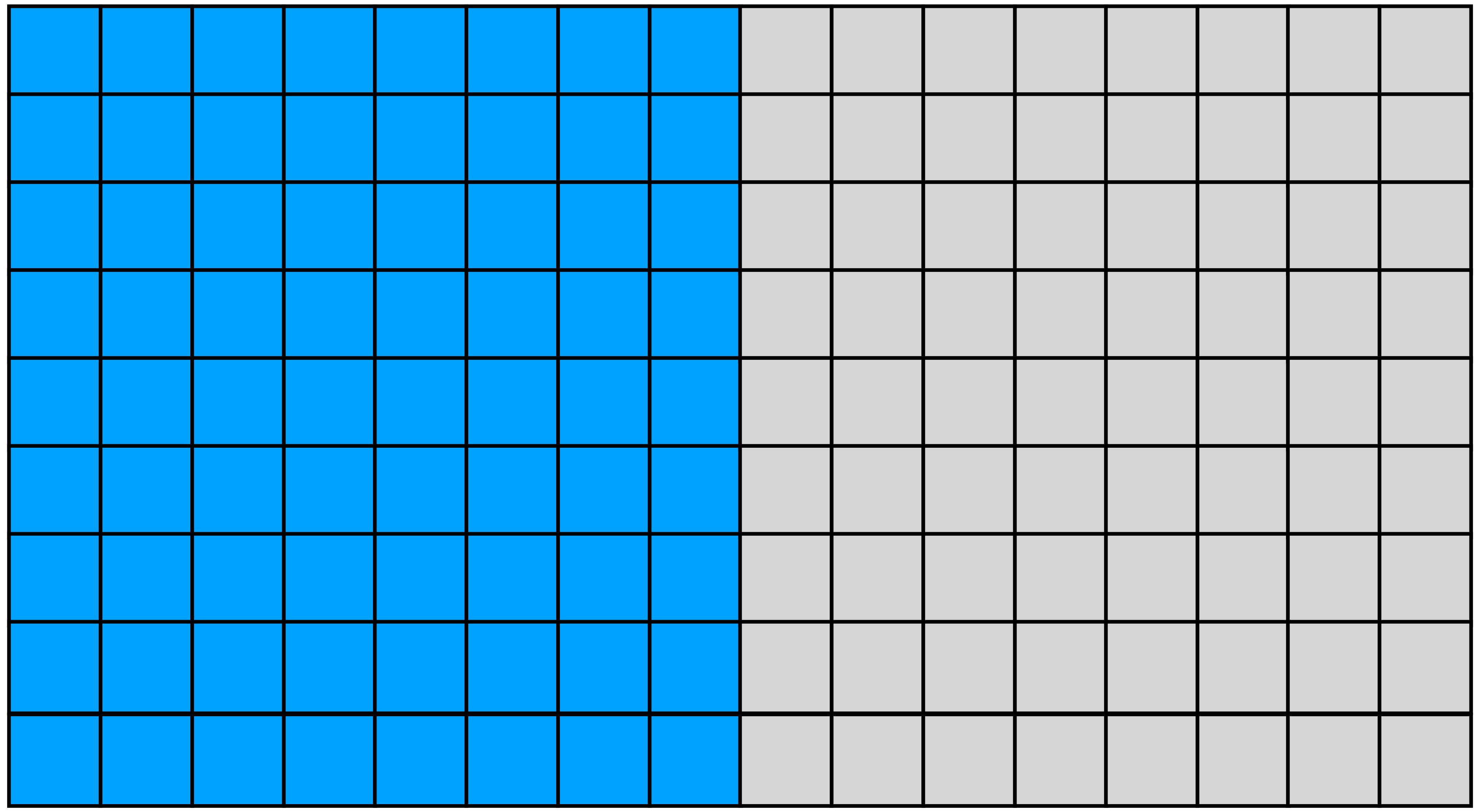
n columns (variable)



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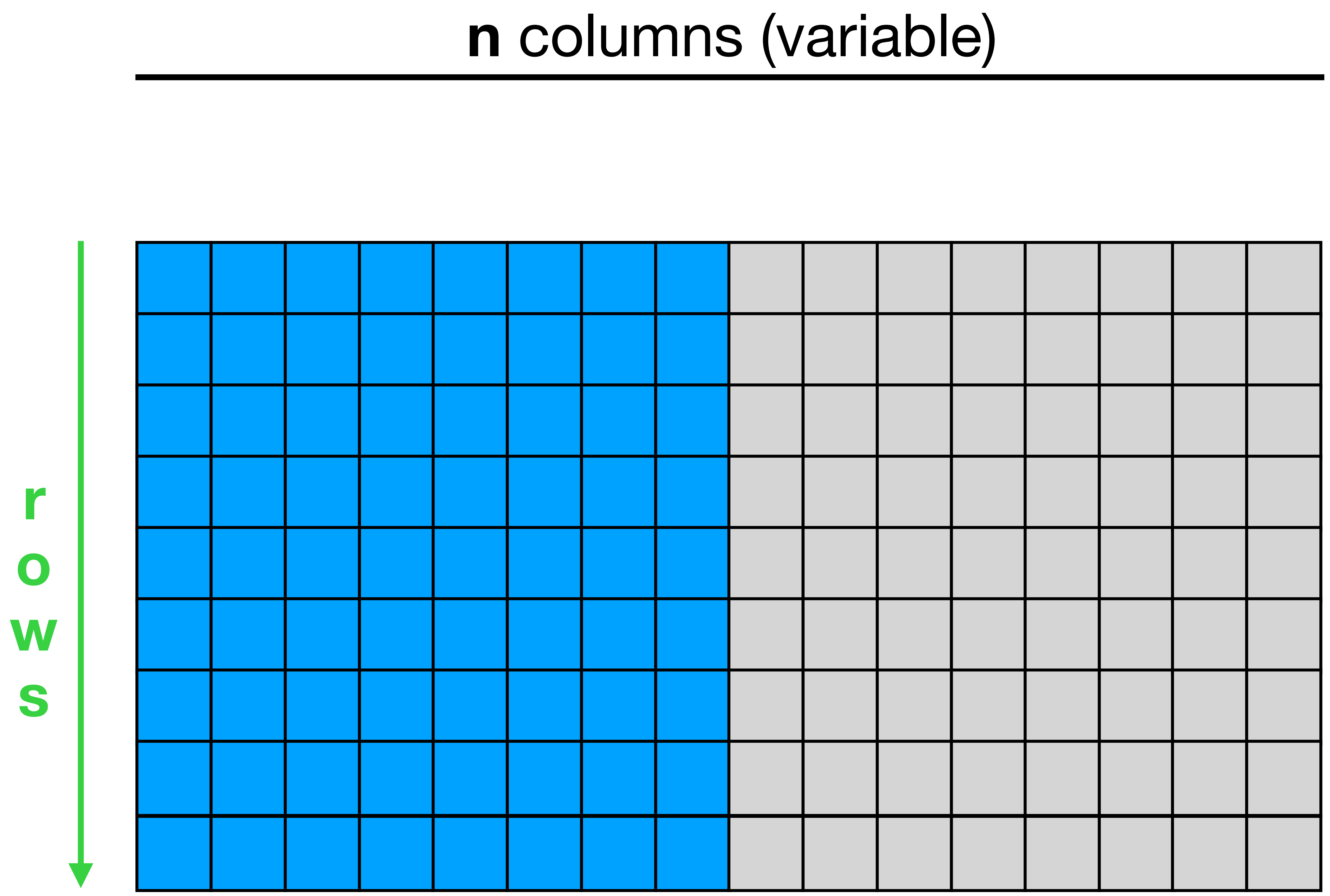

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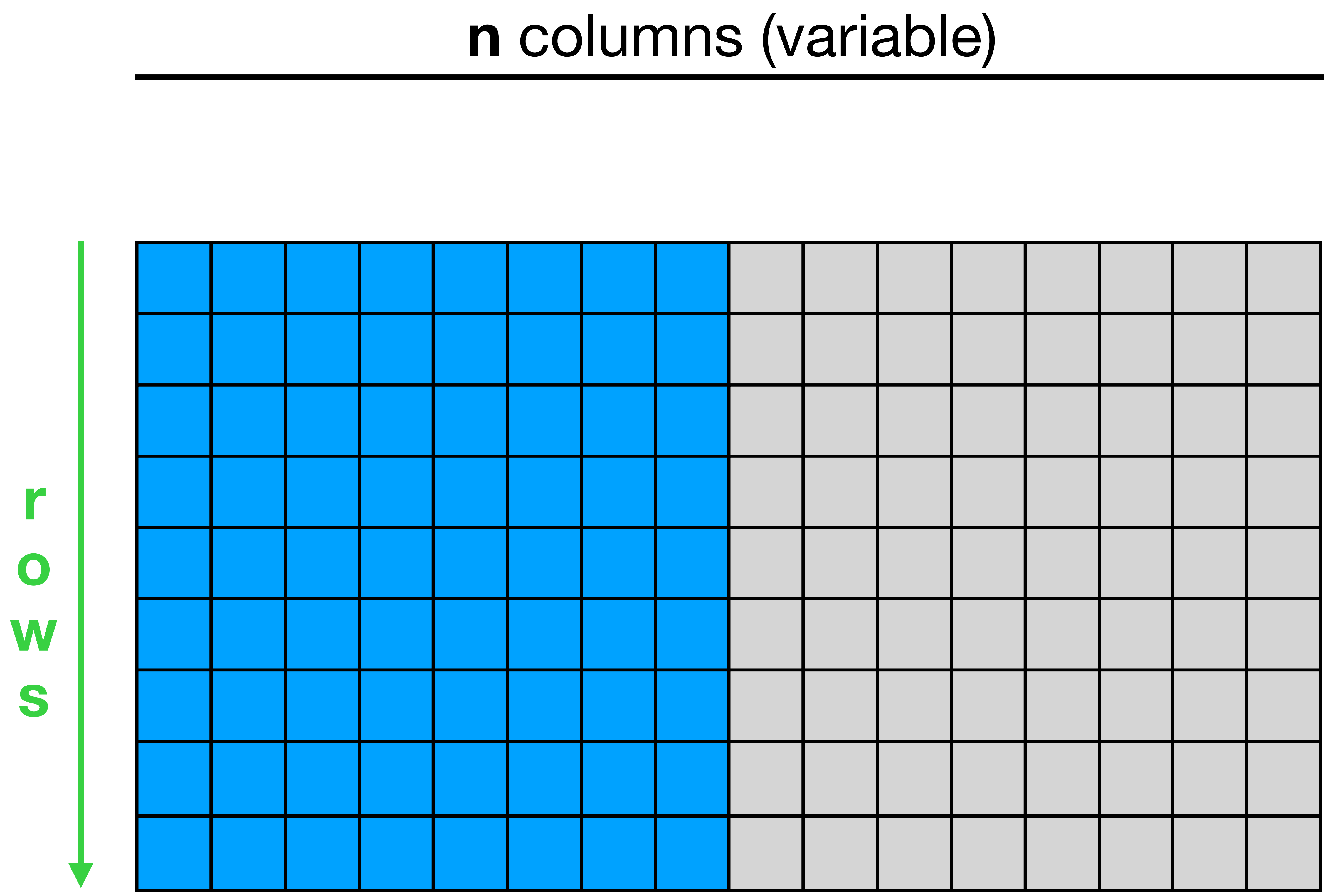
- Traverse each row multiple times the first 8 columns only



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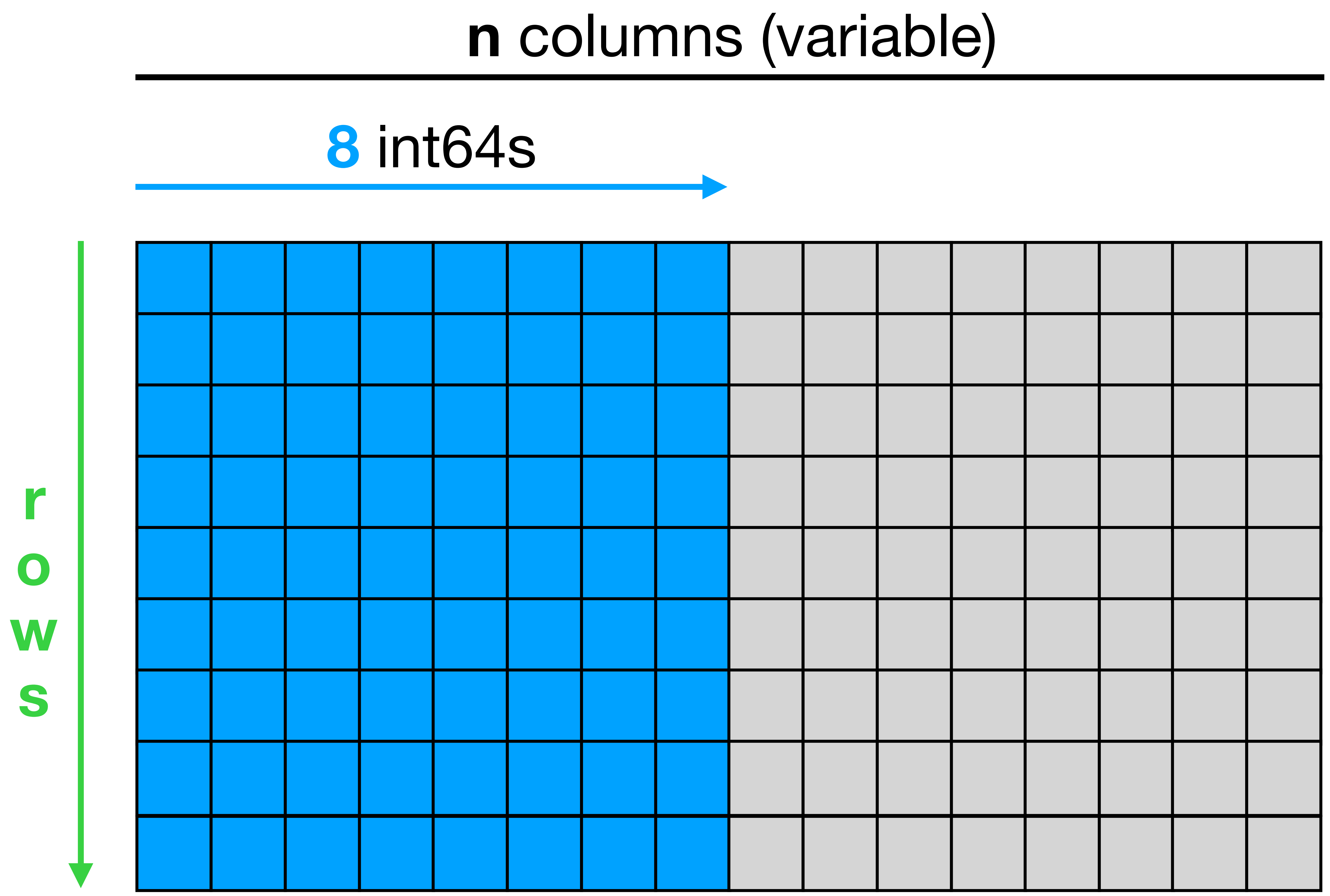

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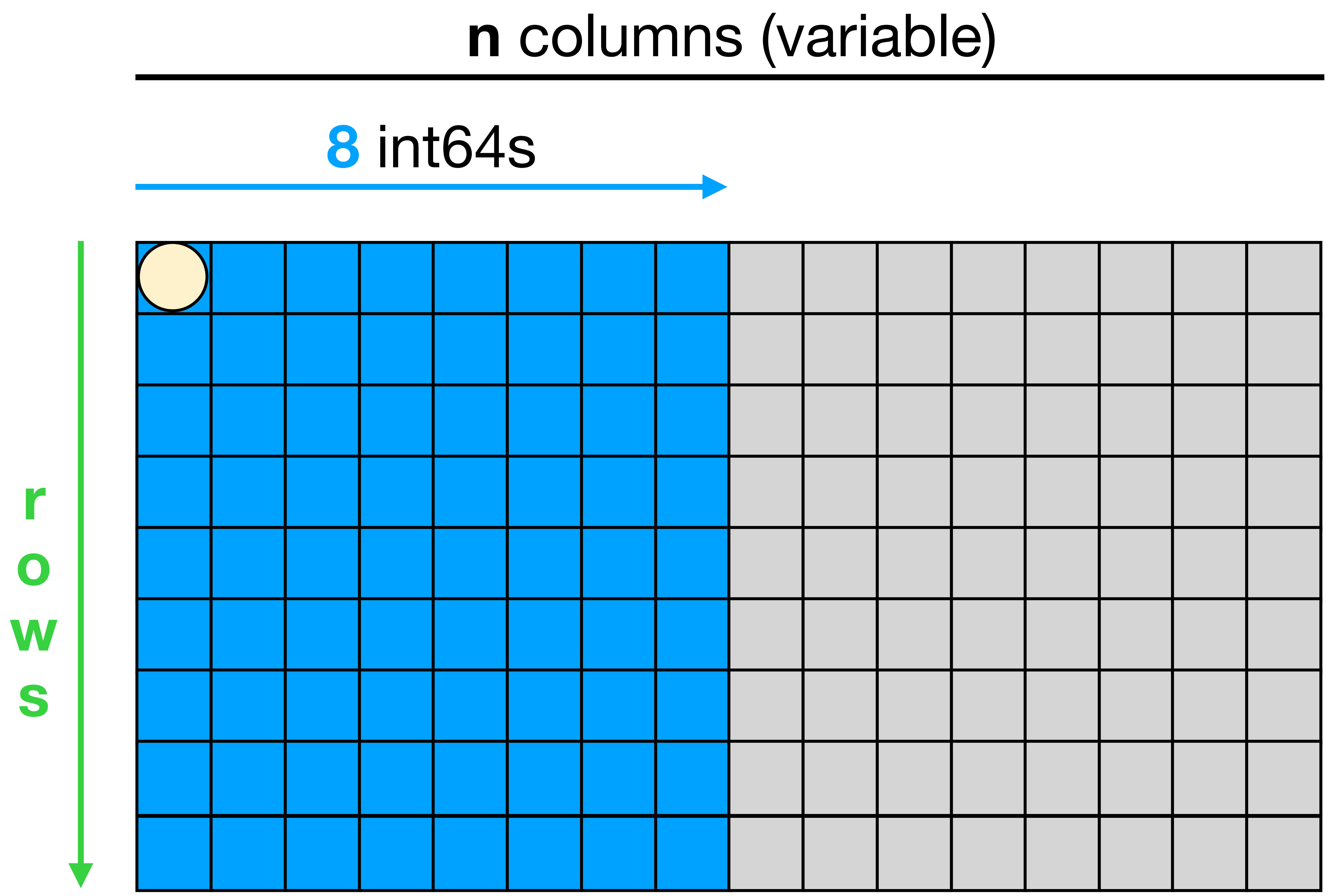

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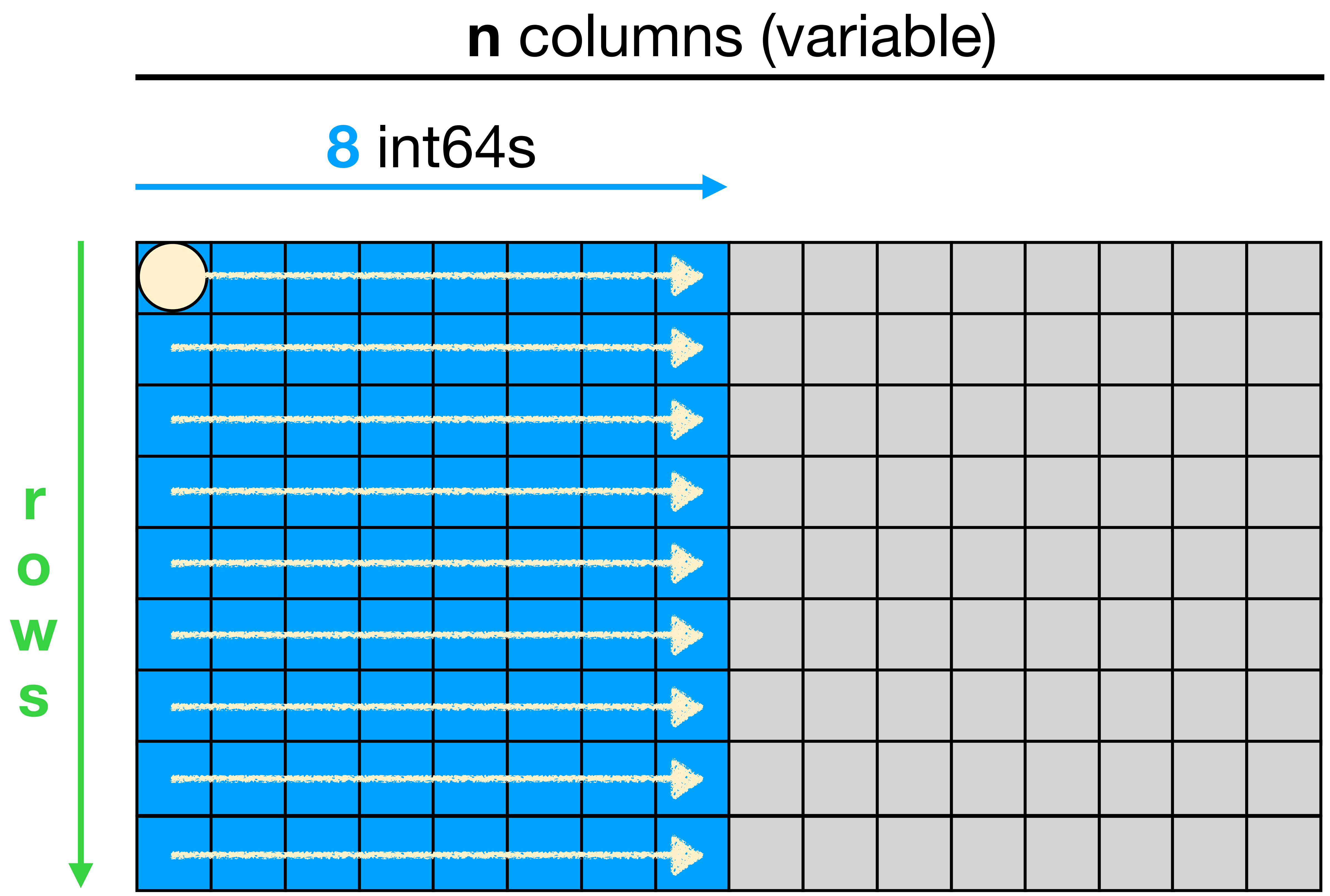

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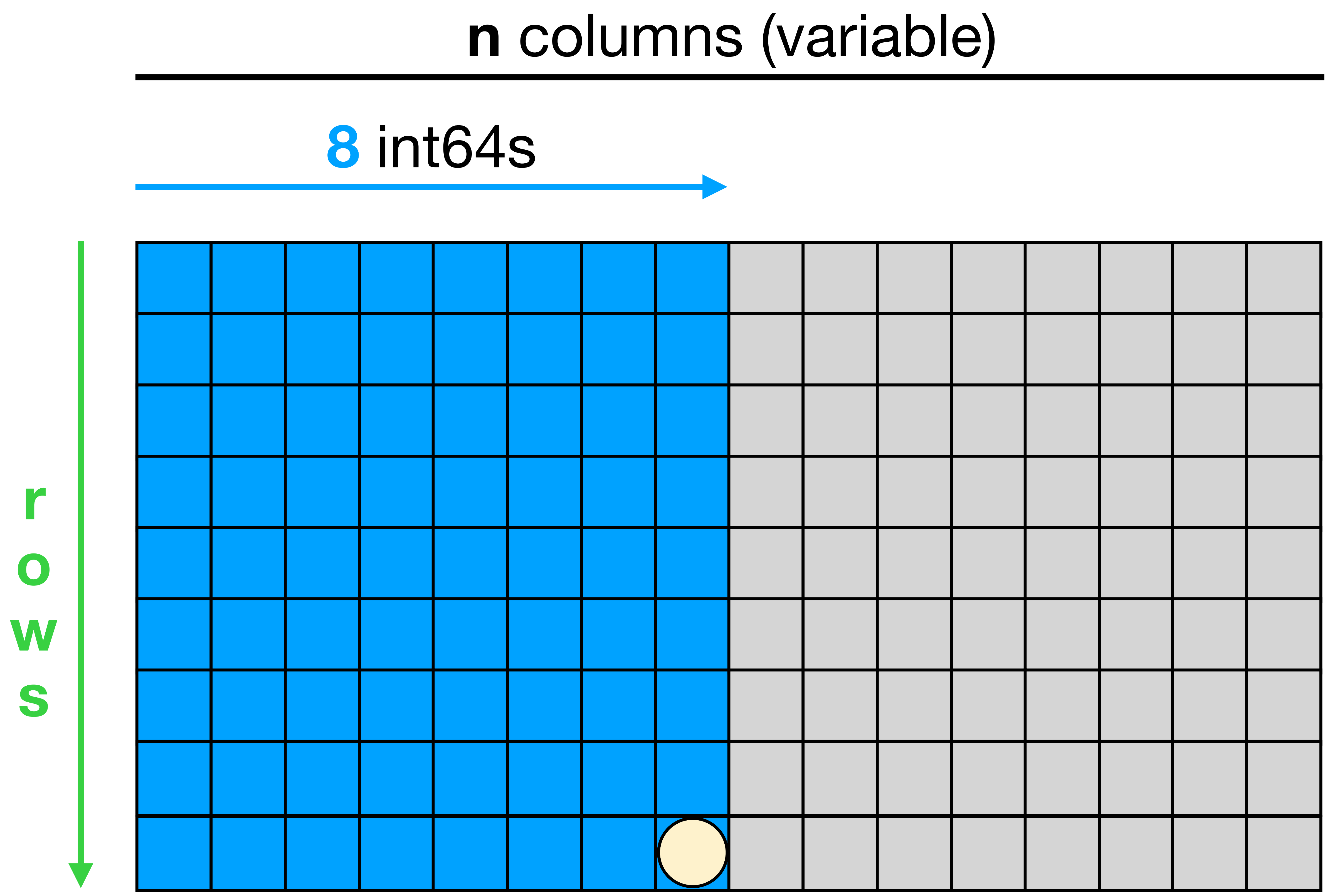

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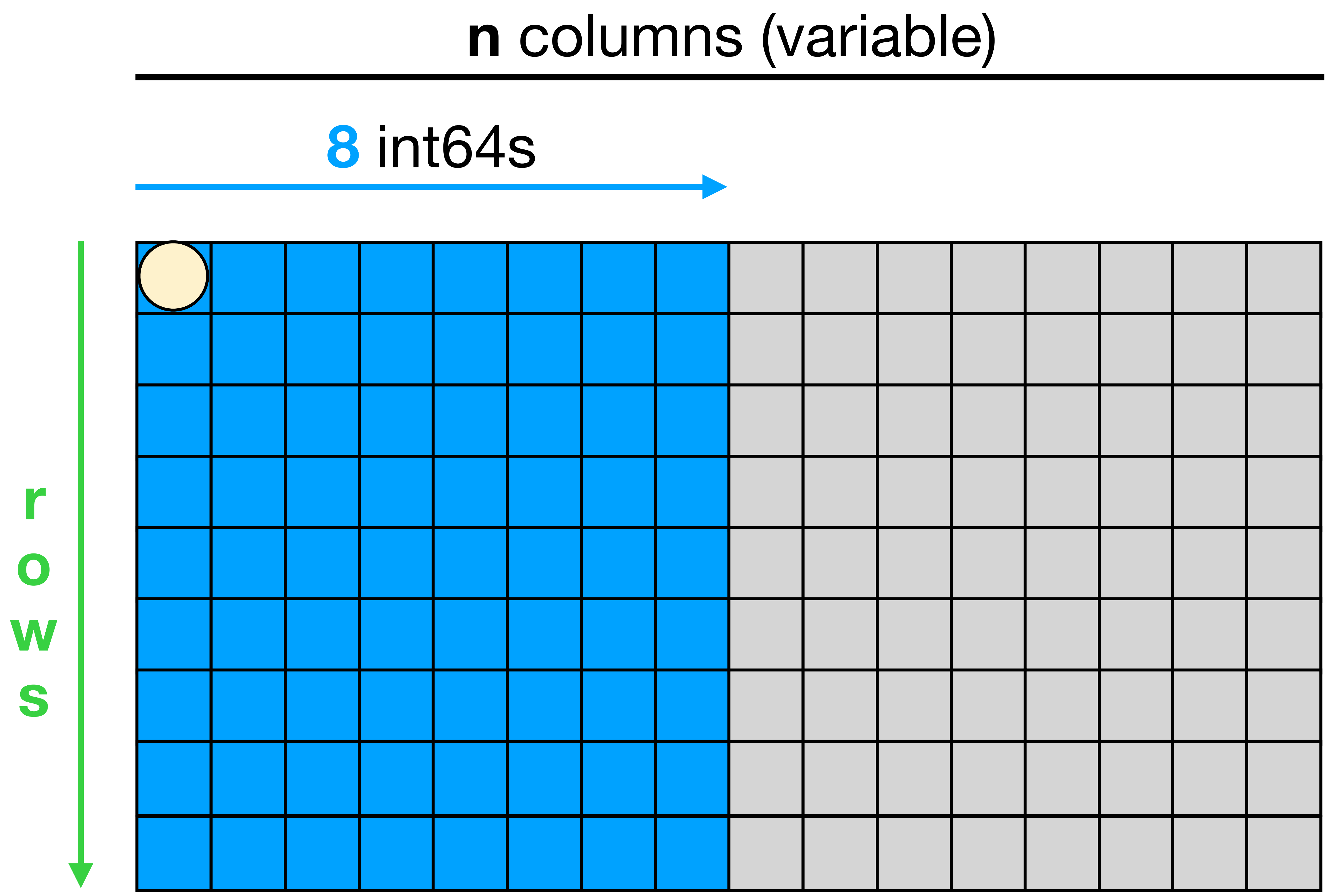

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for 0..k {
    for i in 0..rows {
        for j in 0..8 {
            sum += a[i][j]
        }
    }
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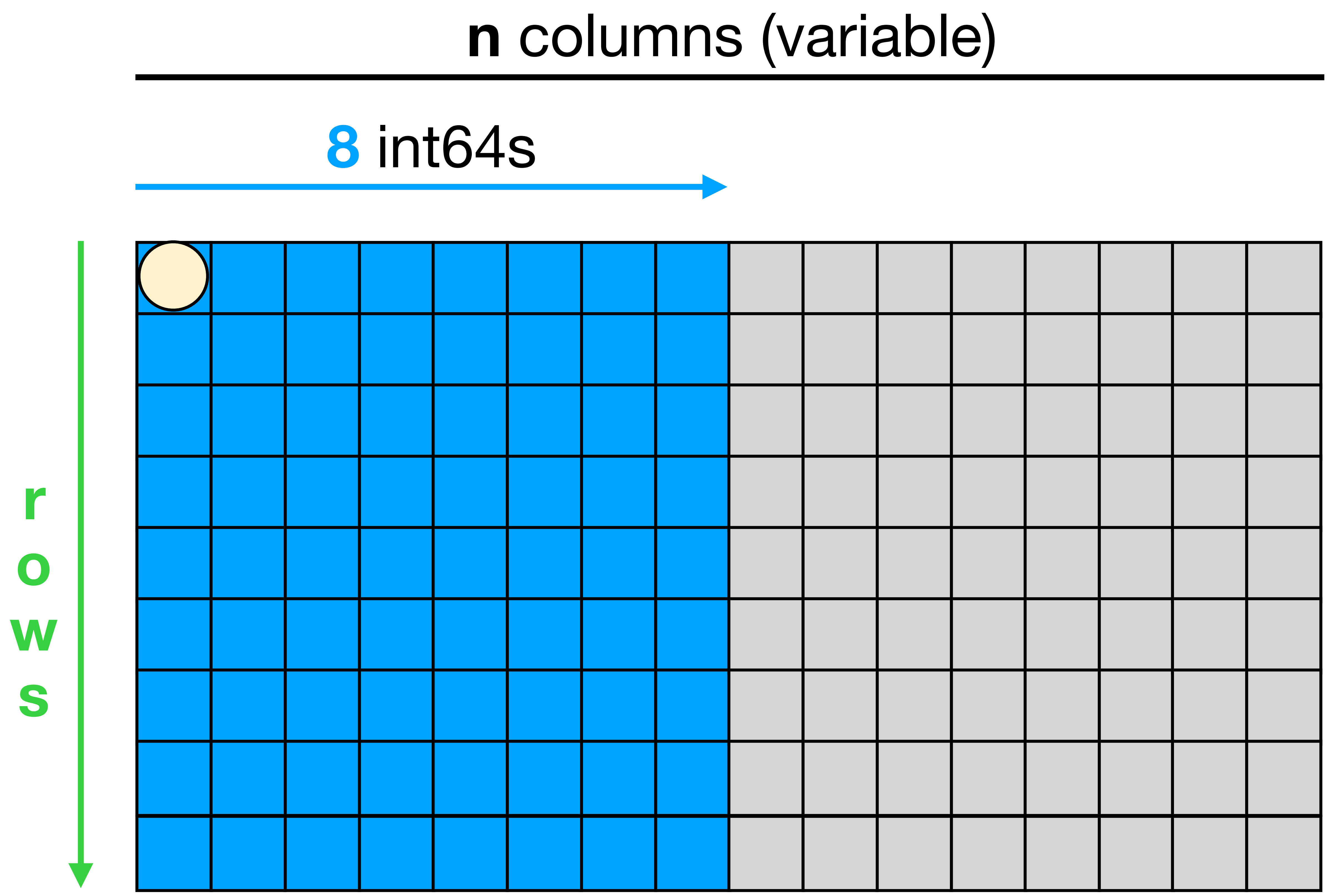

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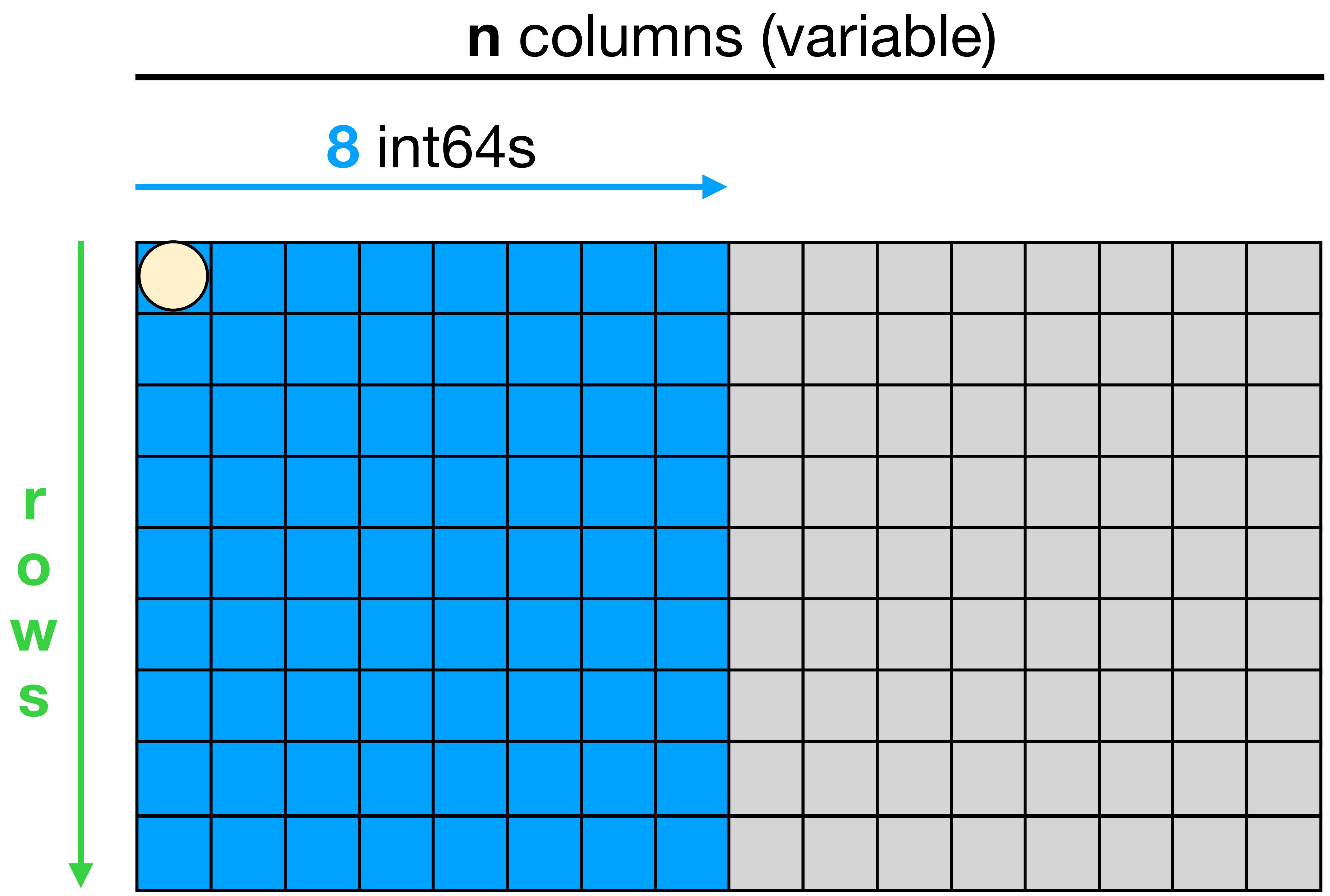

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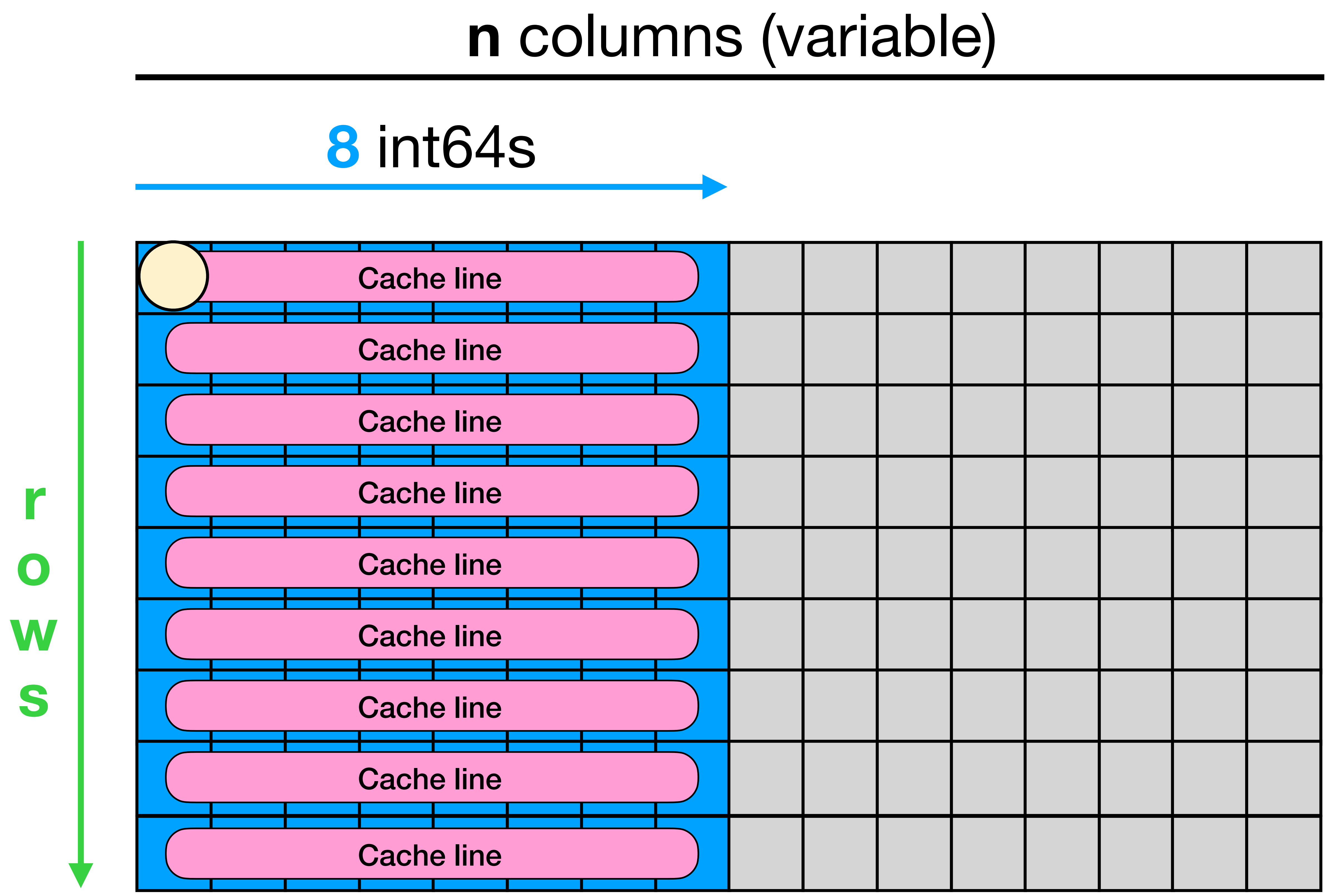

GOPHERCON TURKEY

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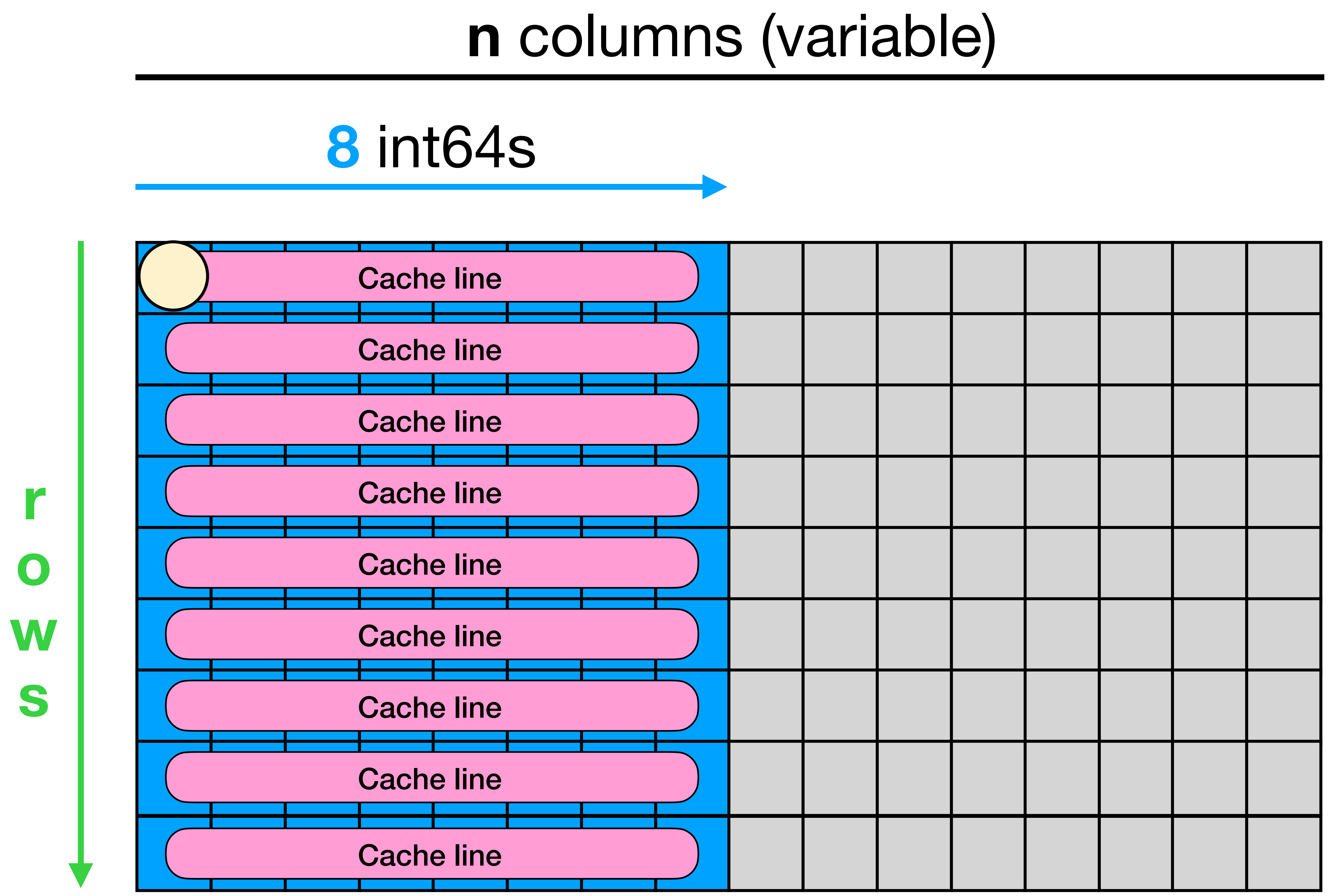
- The execution time depends on **n** (?)



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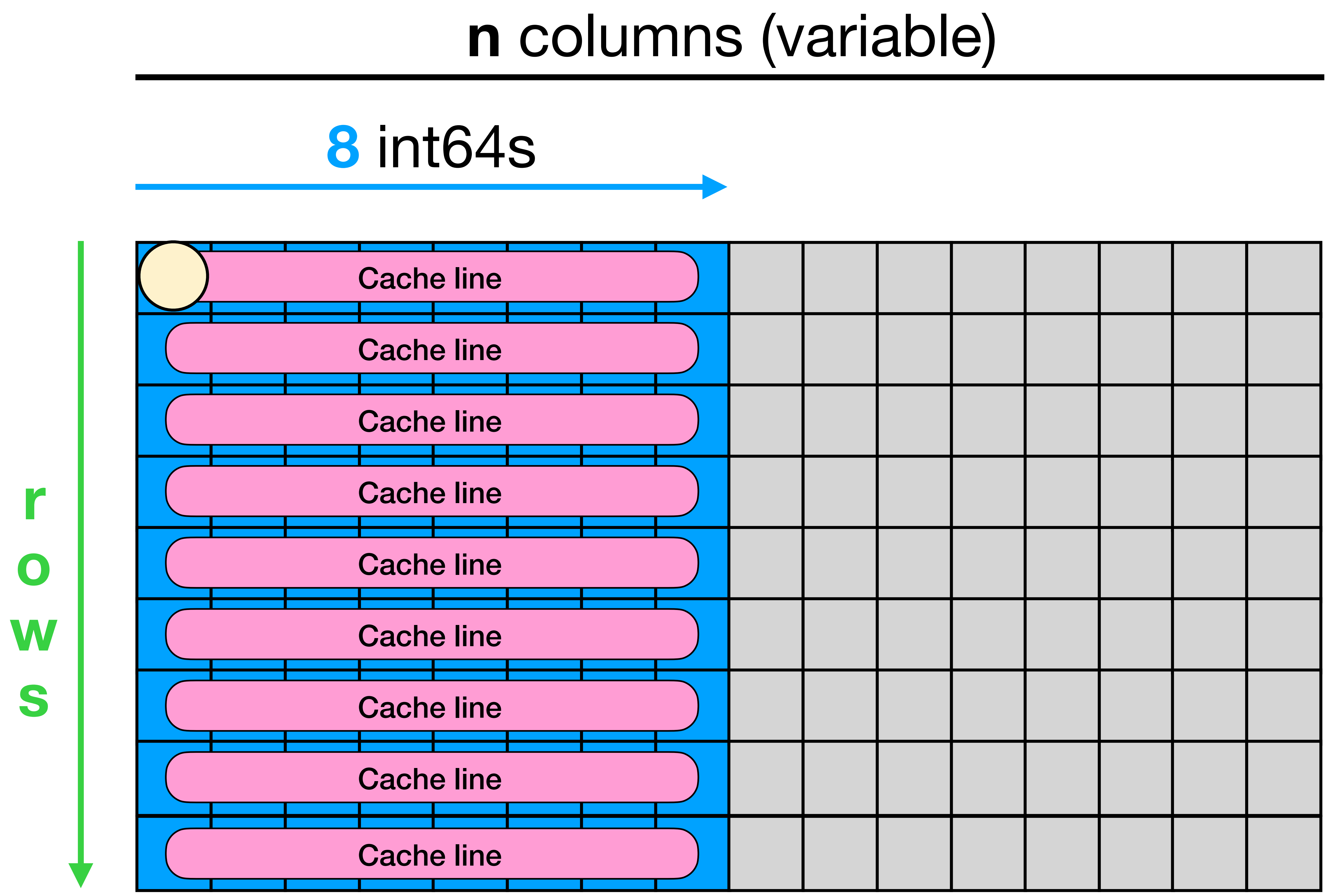
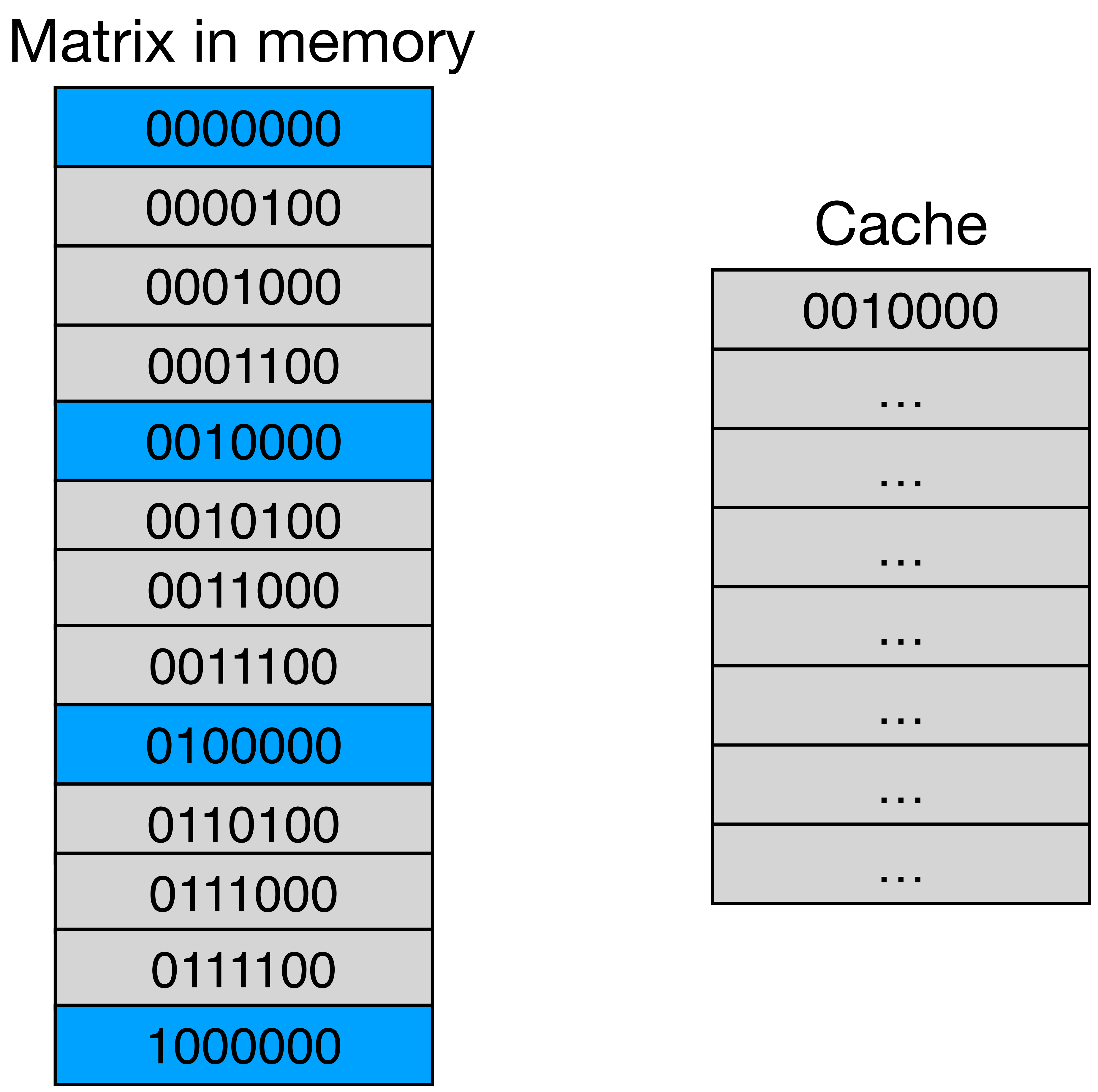
}
```



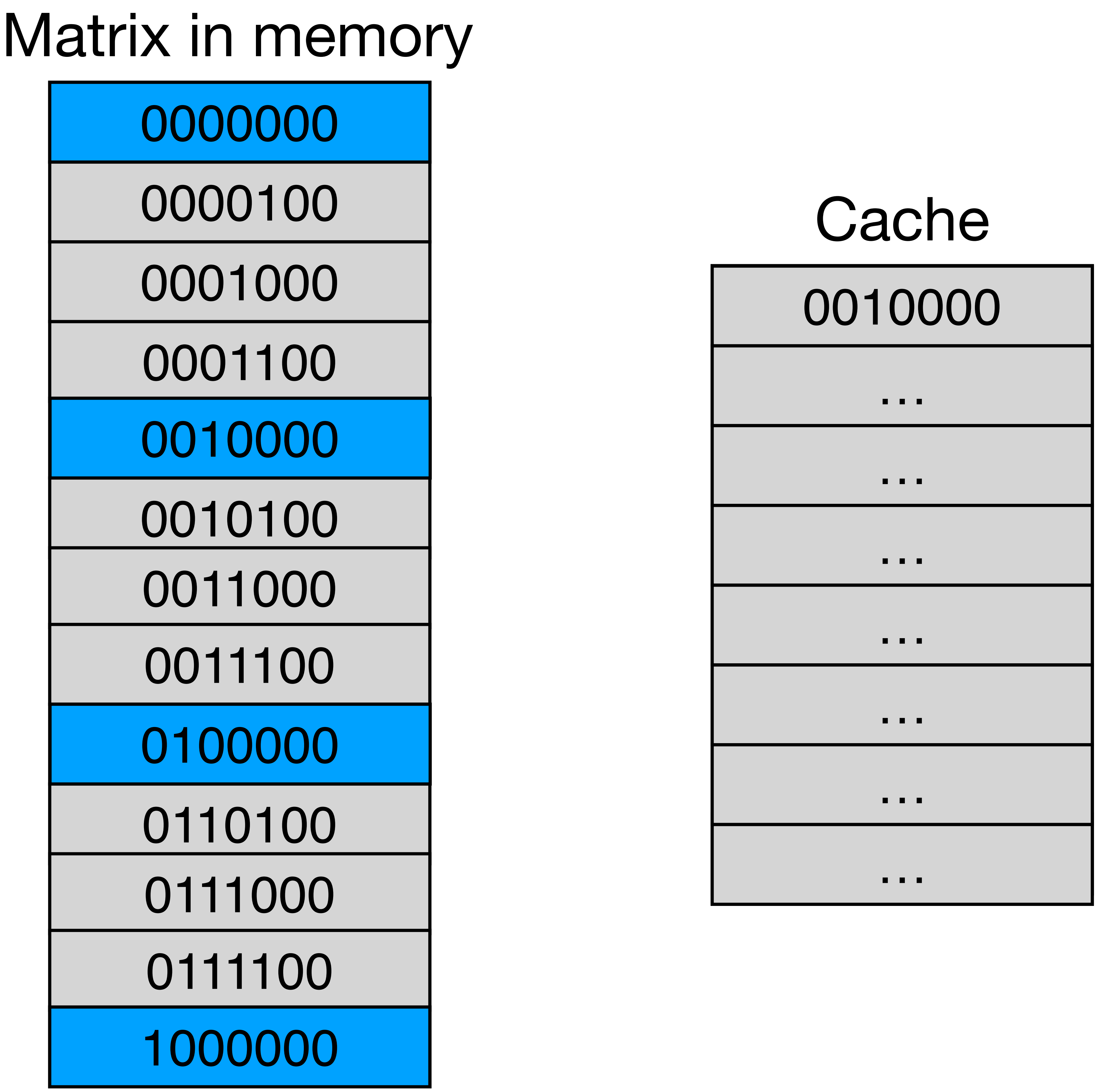
- rows is small enough so that each line should fit in the cache

- The execution time depends on **n** (?)

- Depending on **n**, the execution can be up to **100% slower**

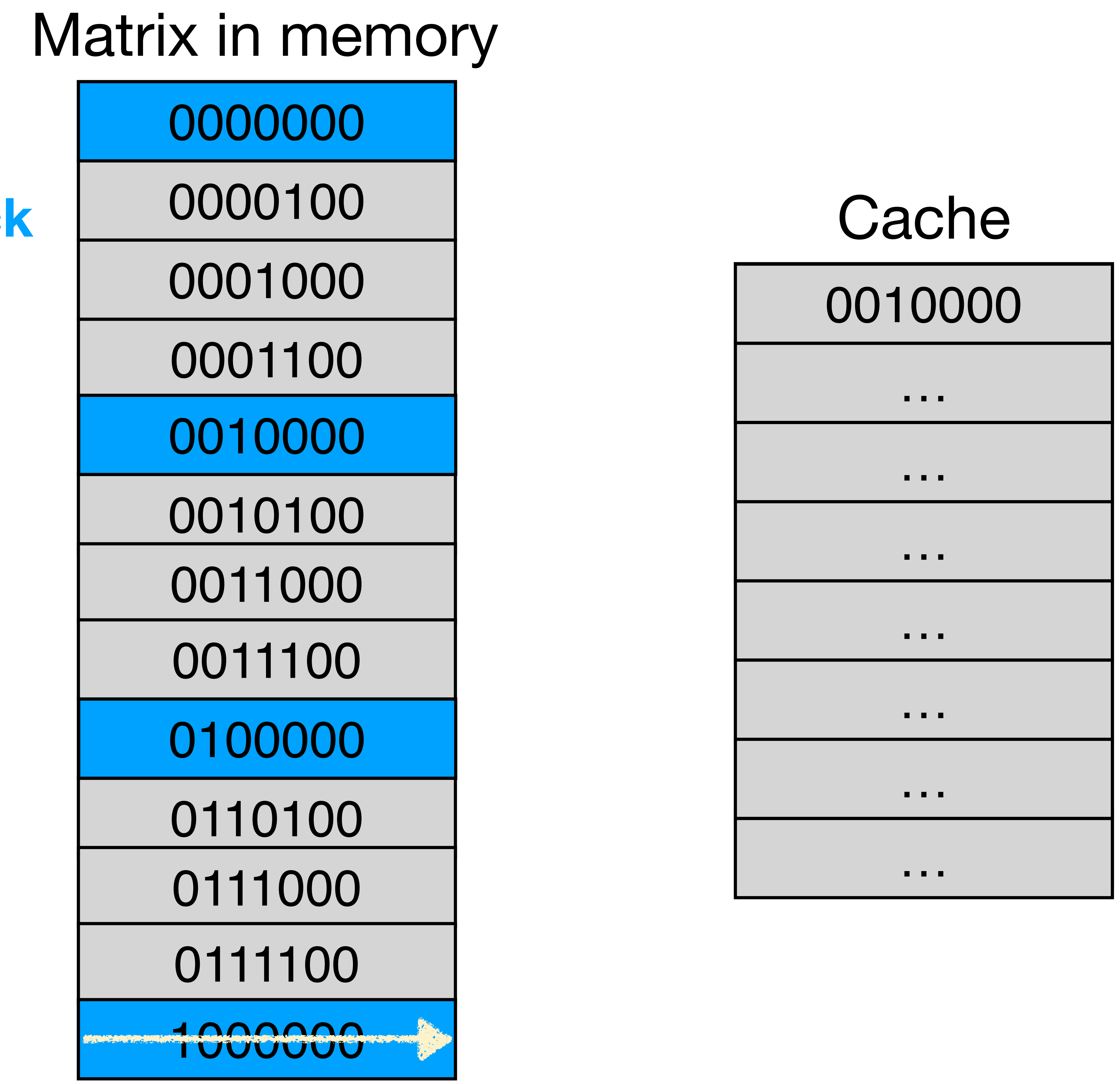

Matrix in memory
0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000
Cache
0010000
...
...
...
...
...
...
...

A block is referenced by an address



A block is referenced by an address

We want to iterate on each **blue block**



A block is referenced by an address

We want to iterate on each **blue block**

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

Cache

0010000
…
…
…
…
…
…
…

Program:

…

load address 0000000

…

A block is referenced by an address

We want to iterate on each **blue block**

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

Cache

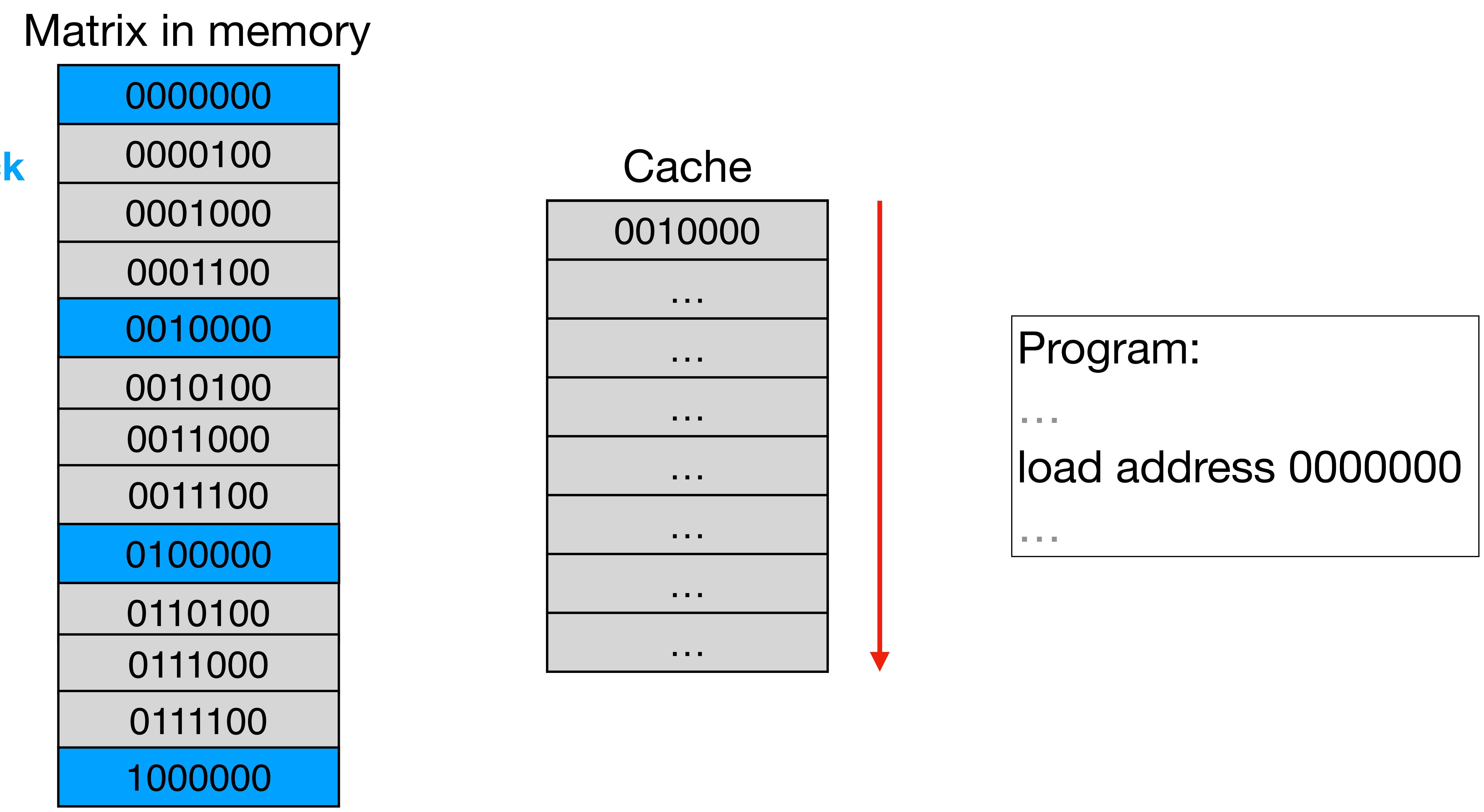
0010000
…
…
…
…
…
…
…

Program:
…
load address 0000000
…

- In a **fully associative cache**, we may have to traverse the **whole** cache to check if an address is present

A block is referenced by an address

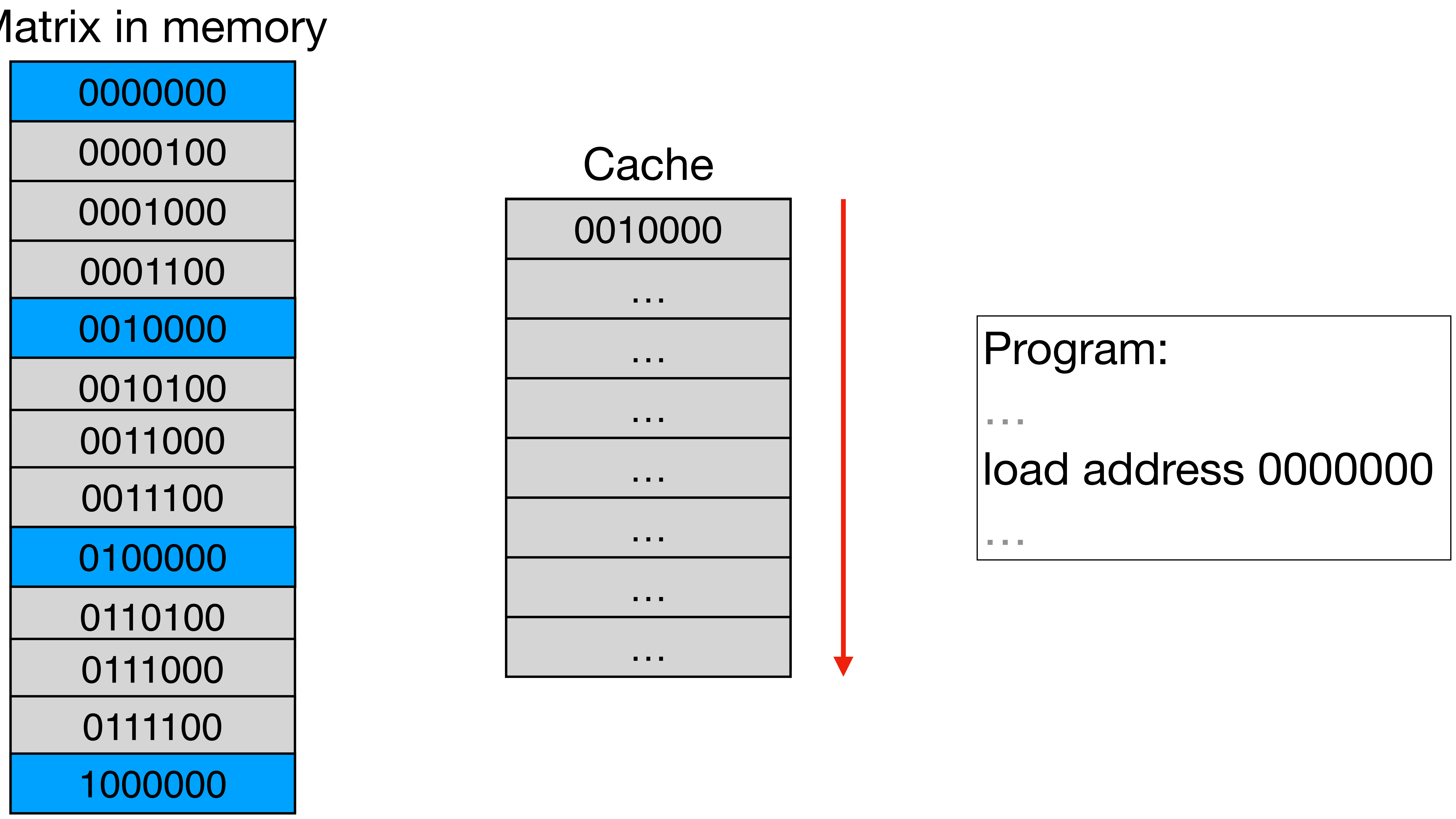
We want to iterate on each **blue block**



- In a **fully associative cache**, we may have to traverse the **whole** cache to check if an address is present

A block is referenced by an address

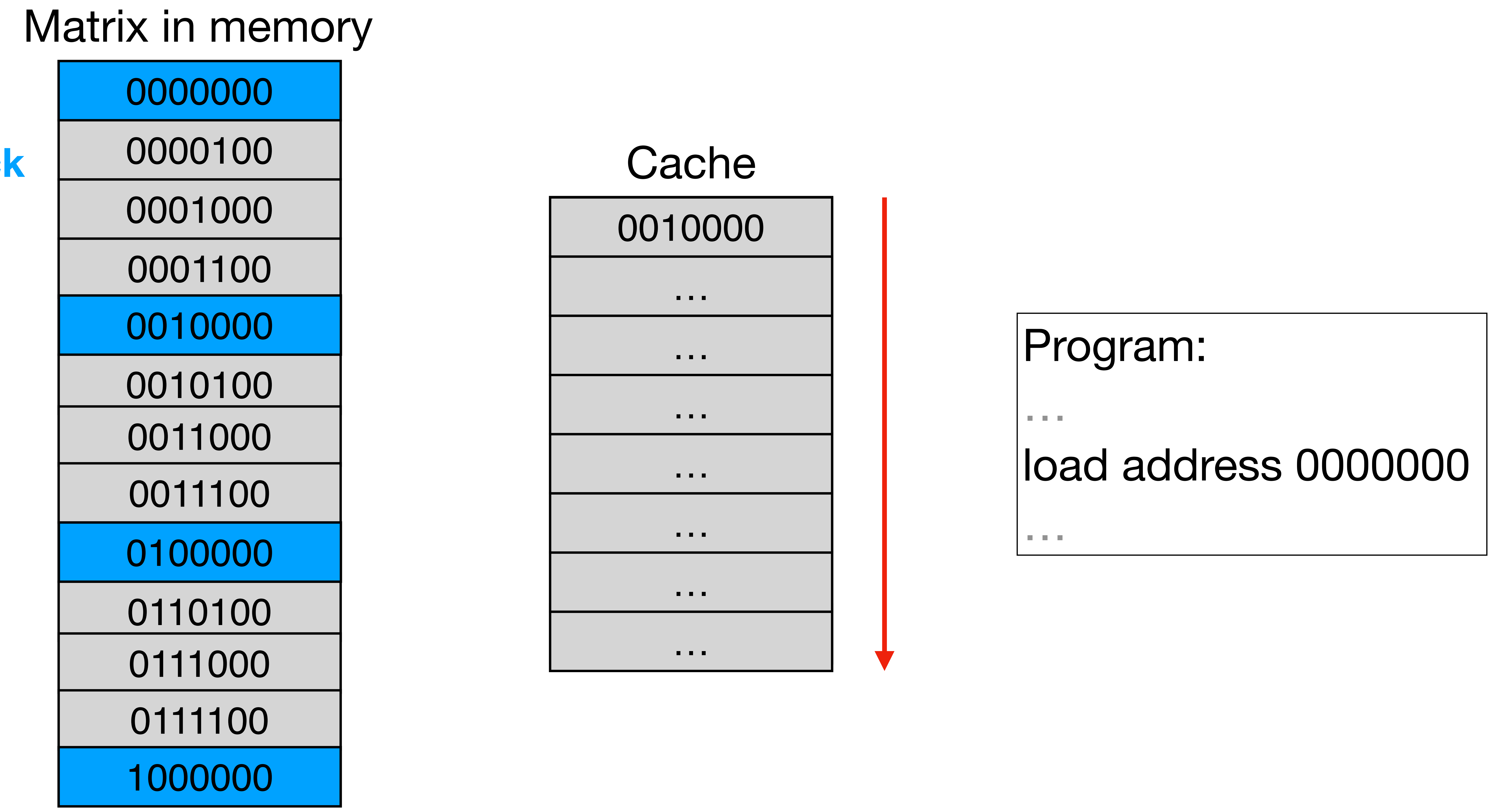
We want to iterate on each **blue block**



- In a **fully associative cache**, we may have to traverse the **whole** cache to check if an address is present
- Example on an Intel Core i5-7300 L1D: we need to iterate on **512 lines**

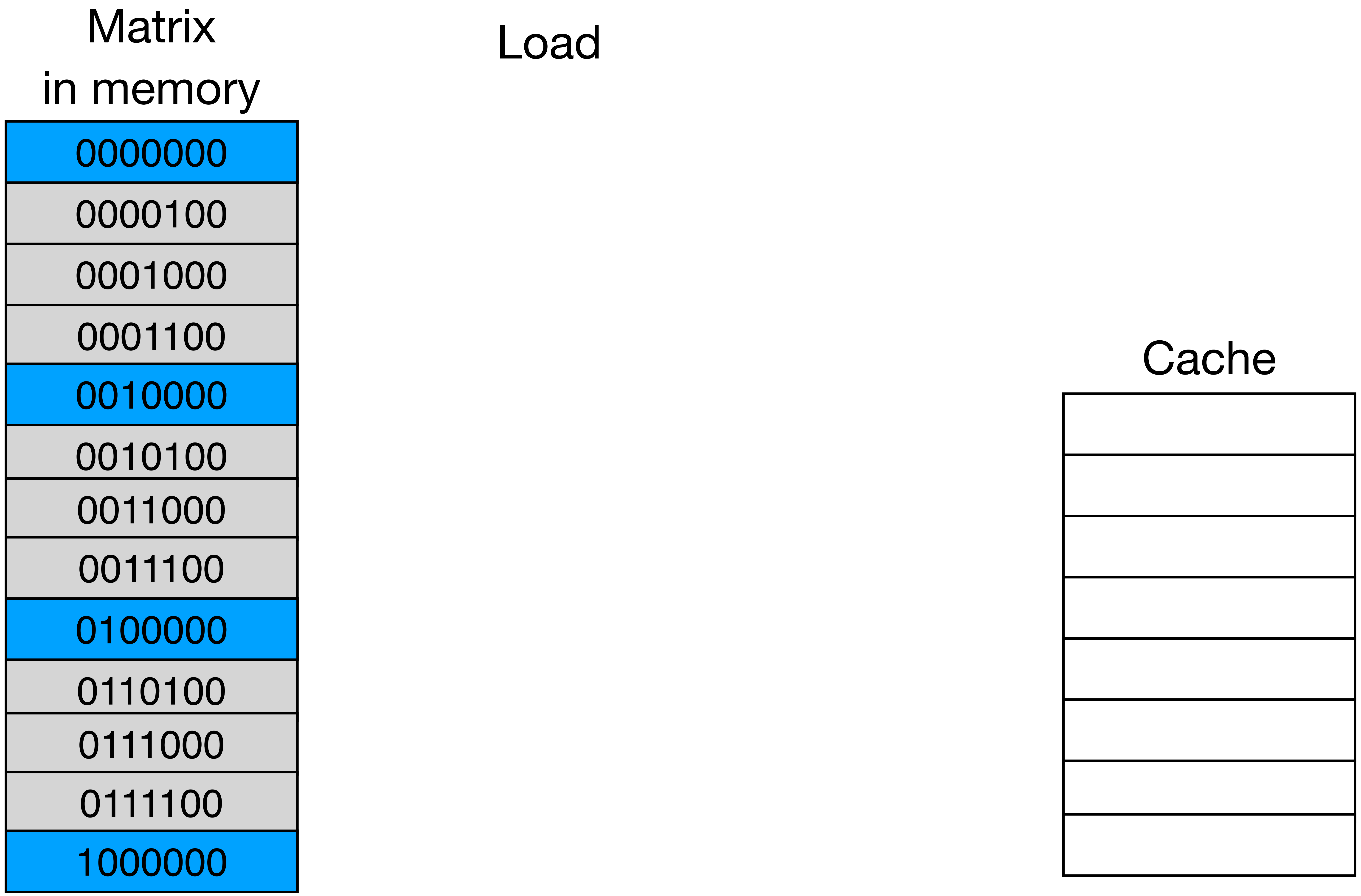
A block is referenced by an address

We want to iterate on each **blue block**



- In a **fully associative cache**, we may have to traverse the **whole** cache to check if an address is present
- Example on an Intel Core i5-7300 L1D: we need to iterate on **512 lines**
- Solution: **partitioning**

Load


Matrix
in memory
0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000
Cache

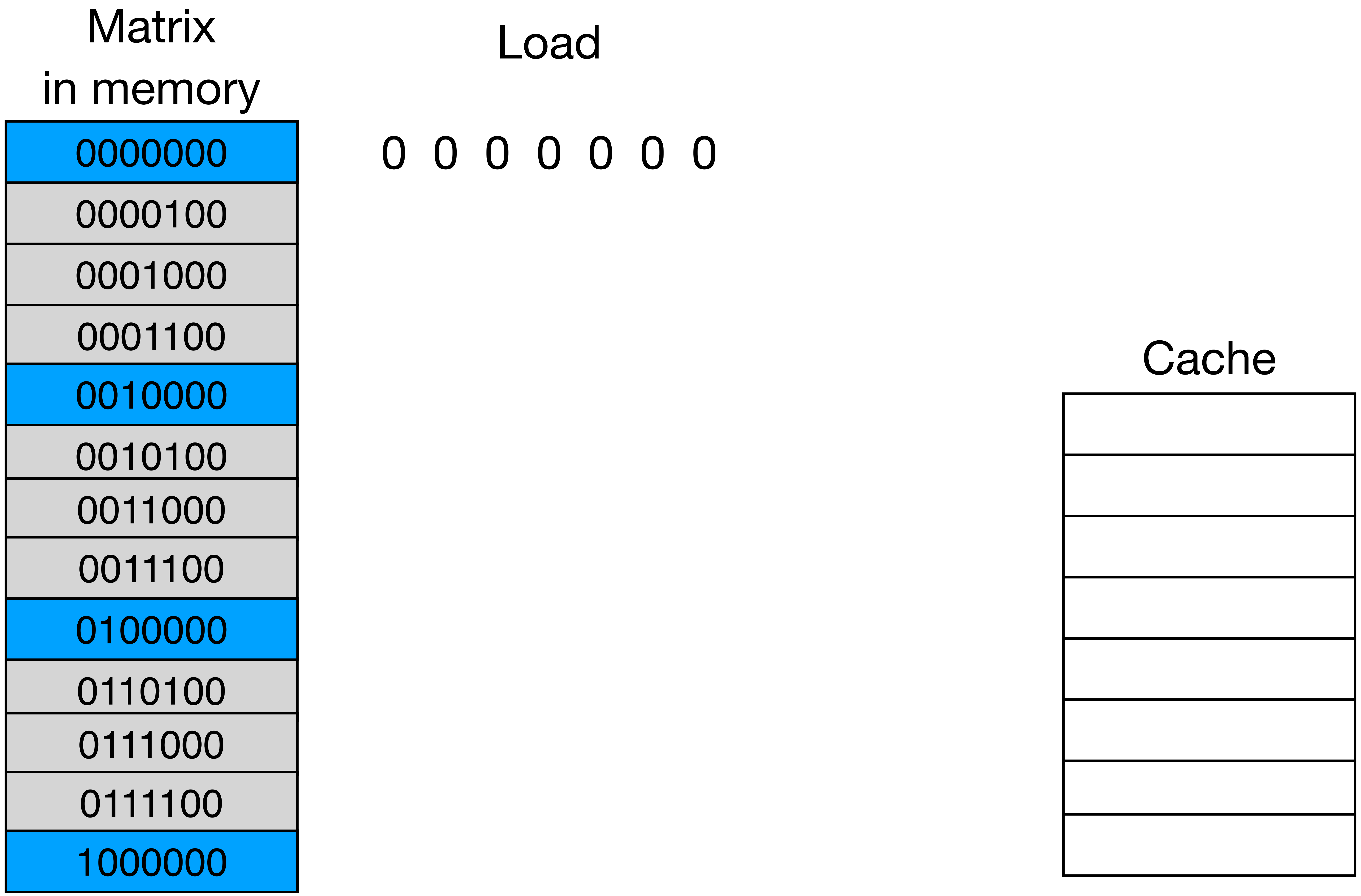
Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

Load

0 0 0 0 0 0 0

Cache



E.g Block size: 4 bits

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

Load

0 0 0 0 0 0 0

Cache

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

Load

0 0 0 0 0 0 0

bo

Cache

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

GOPHERCON TURKEY

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

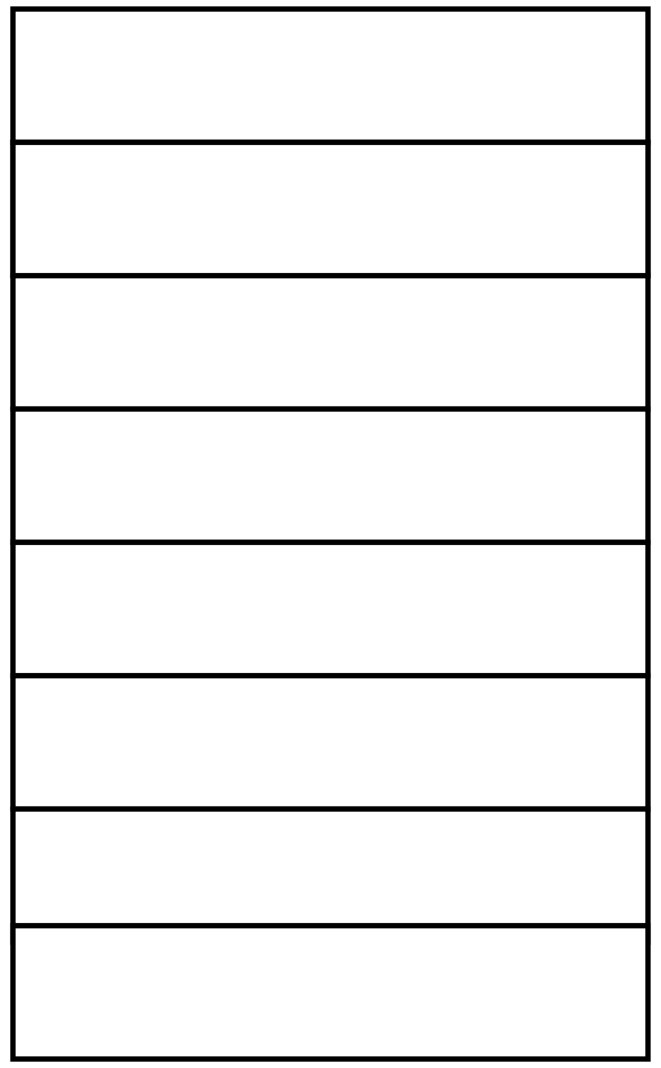
Load

0 0 0 0 0 0 0

bo

A cache is **partitioned** into **sets**

Cache



Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

Load

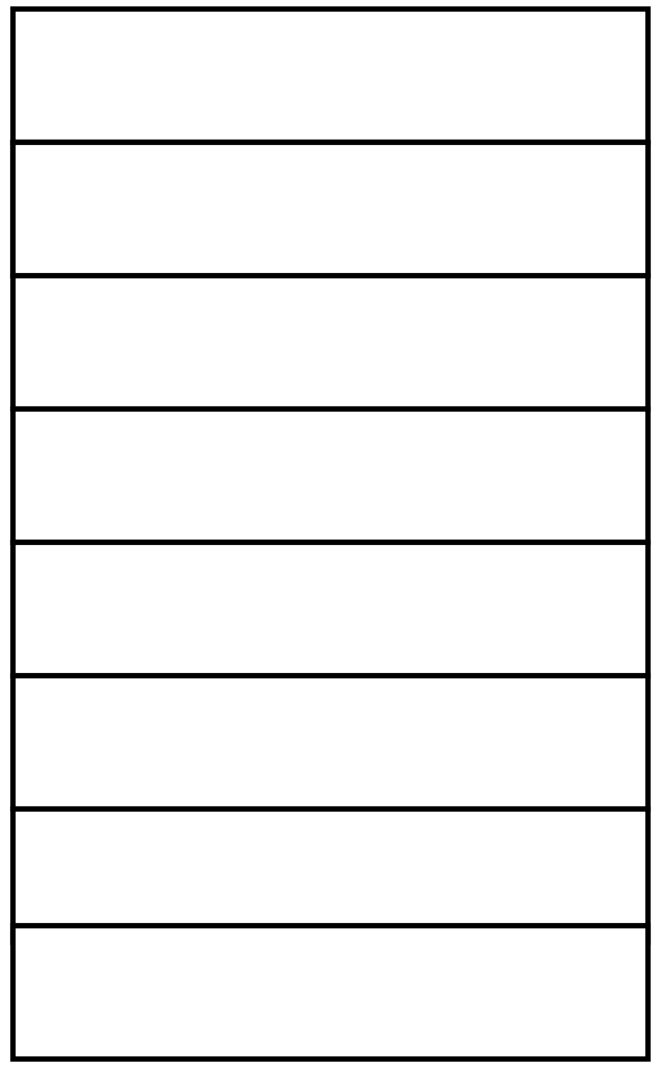
0 0 0 0 0 0 0

bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

Cache



Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the

block offset (bo)

Load

0 0 0 0 0 0 0

bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

Cache

Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the

block offset (bo)

Load

0 0 0 0 0 0 0

bo

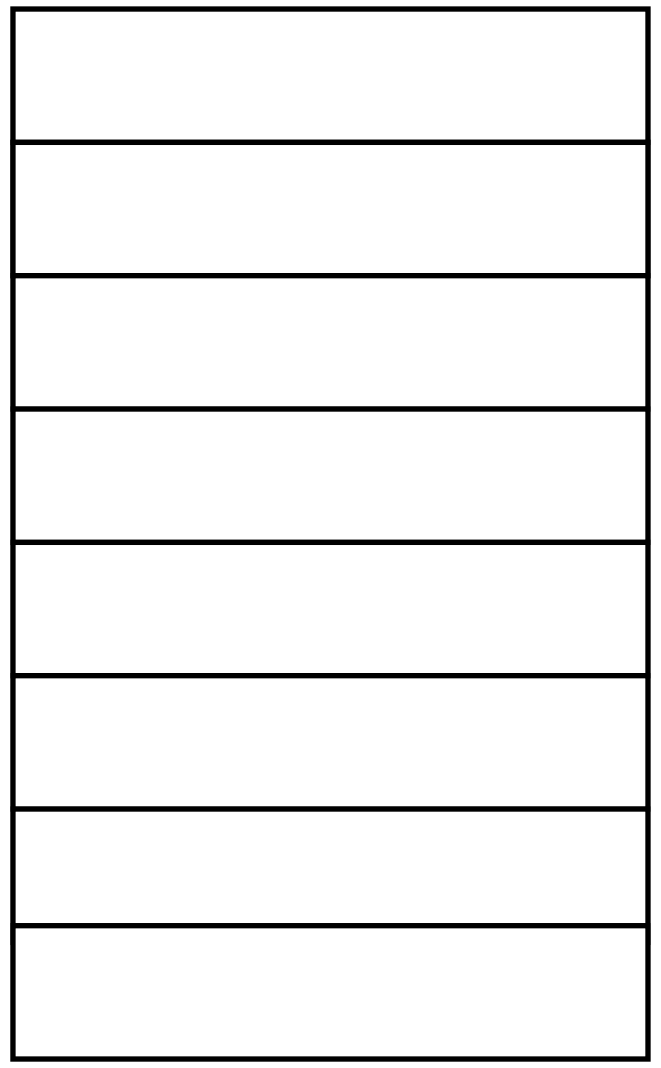
A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

Cache



GOPHERCON TURKEY

Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

Load

0 0 0 0 0 0 0

bo

A cache is **partitioned** into **sets**

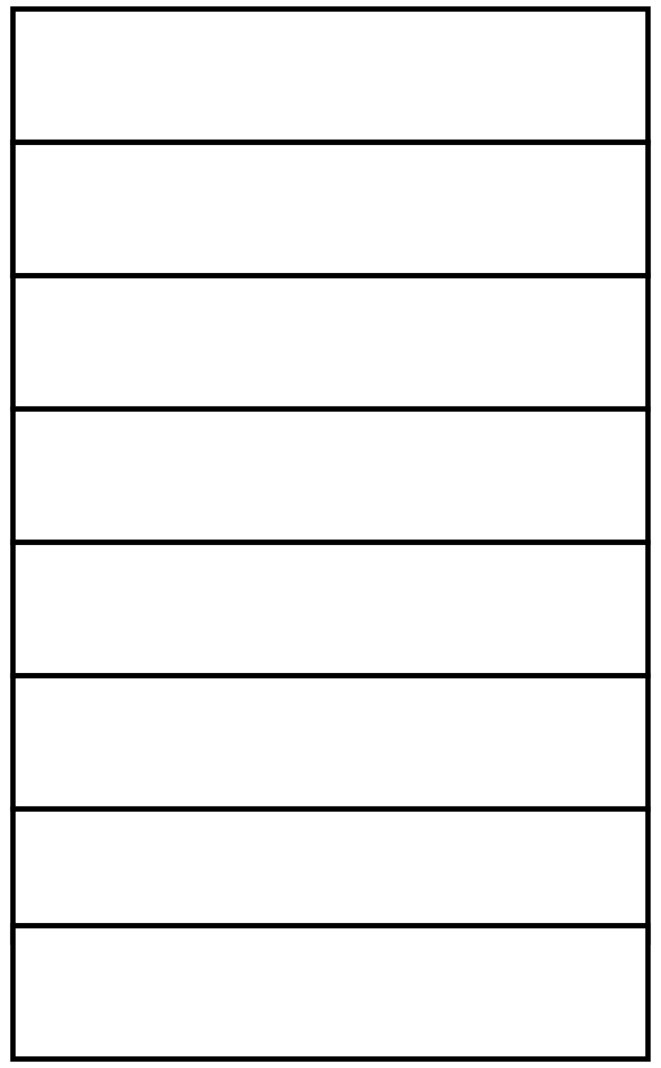
A block can belong to **only one** set

k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

Cache



Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the

block offset (bo)

Load

0 0 0 0 0 0 0

bo

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E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

0 0 0 0 0 0 0

bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

Cache

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^{2}$

2 represents the **set index** (si)

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

0 0 0 0 0 0 0

si bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

Cache

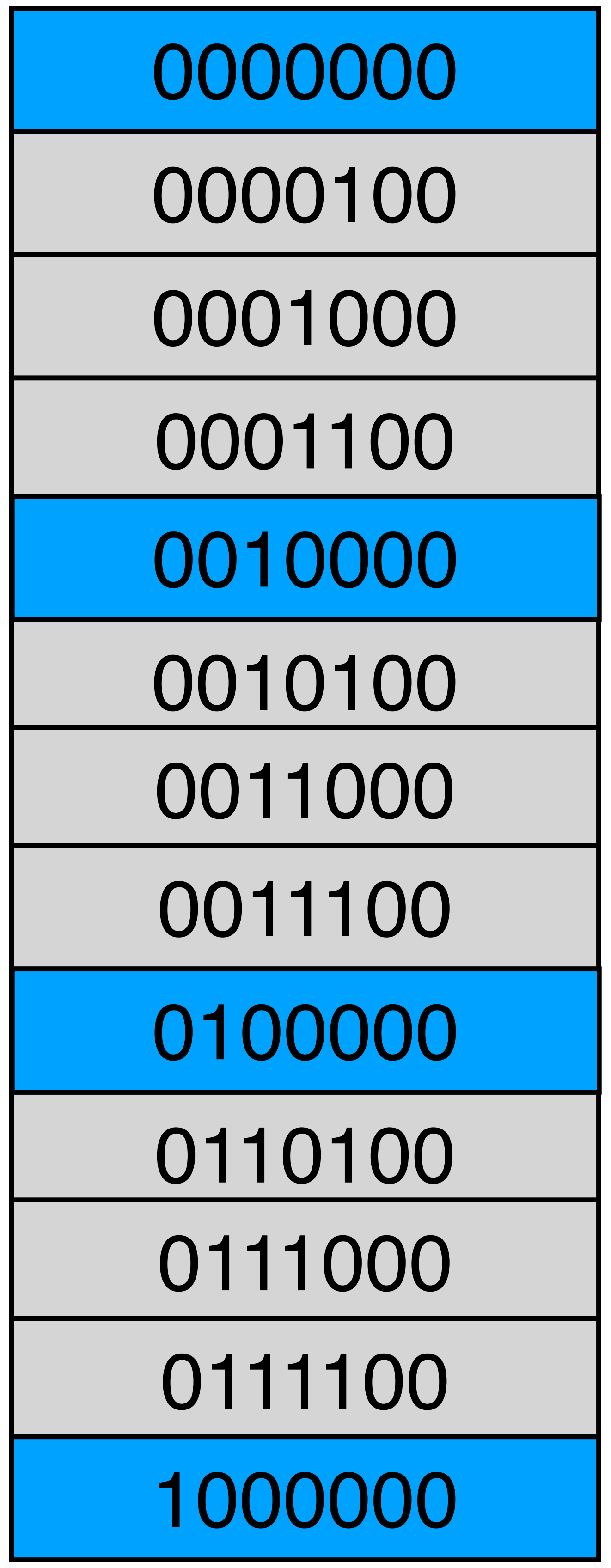
E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^{2}$

2 represents the **set index** (si)

Matrix in memory



E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

This address belongs to set 0

0 0 0 0 0 0 0

si bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

Cache

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^{2}$

2 represents the **set index** (si)

Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

This address belongs to set 0

0 0 0	0 0	0 0
tb	si	bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

Cache

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

This address belongs to set 0

0 0 0 | 0 0 | 0 0

tb | si | bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

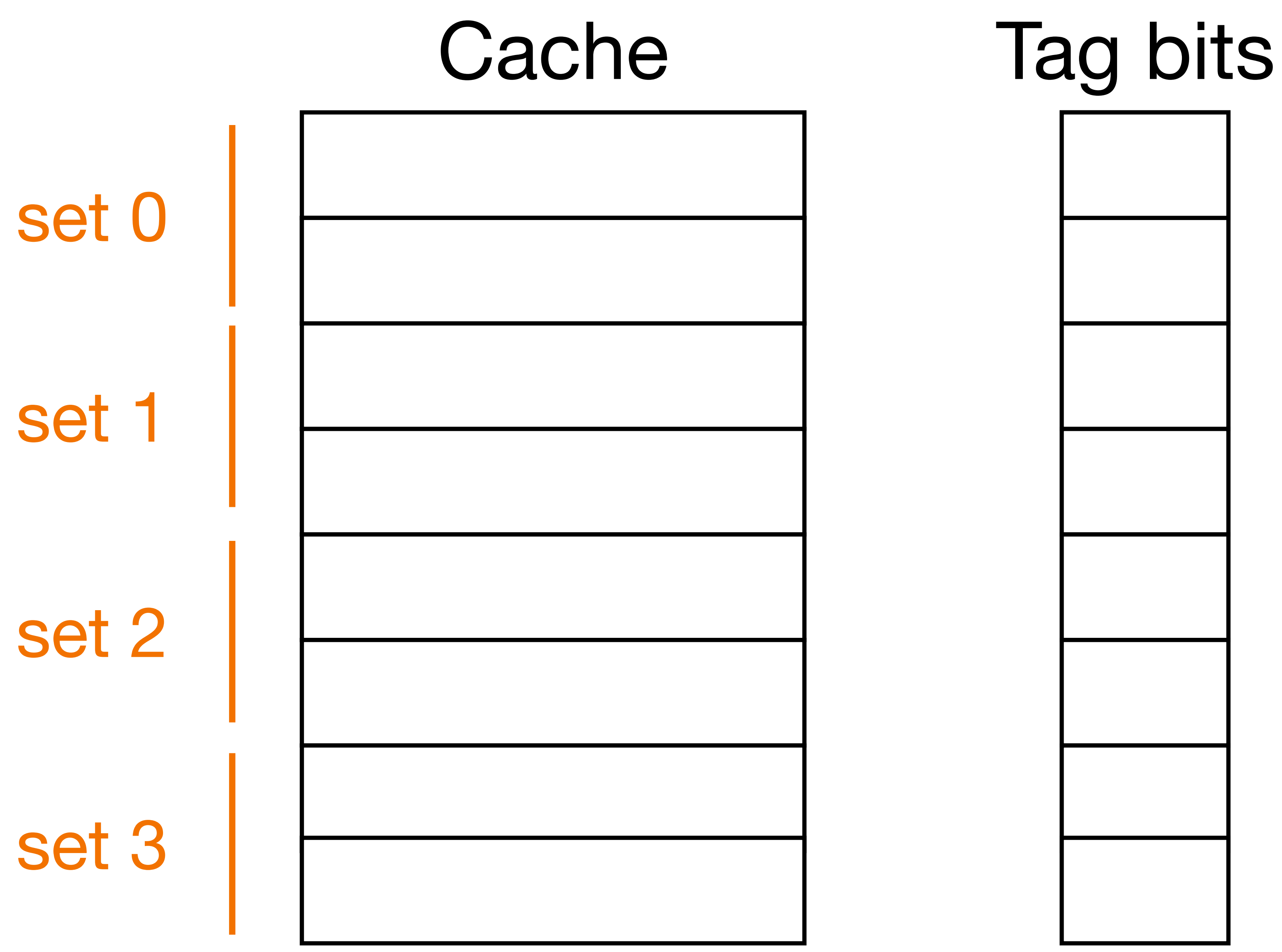
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)



Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

This address belongs to set 0

0 0 0 | 0 0 | 0 0

tb | si | bo

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nb of sets = 8 / 2 = 4

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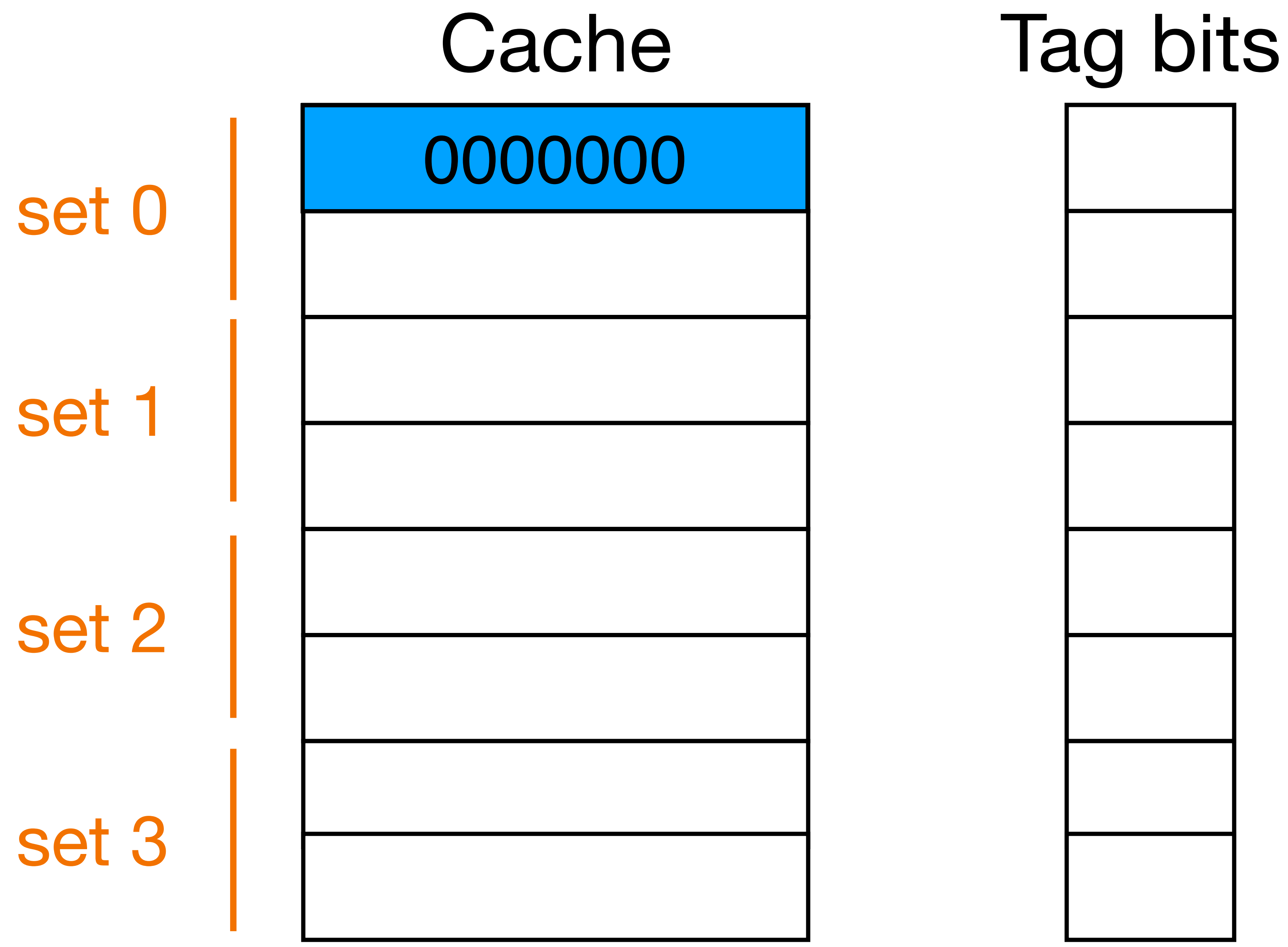
2 represents the **set index** (si)



Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

This address belongs to set 0

0 0 0	0 0	0 0
tb	si	bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

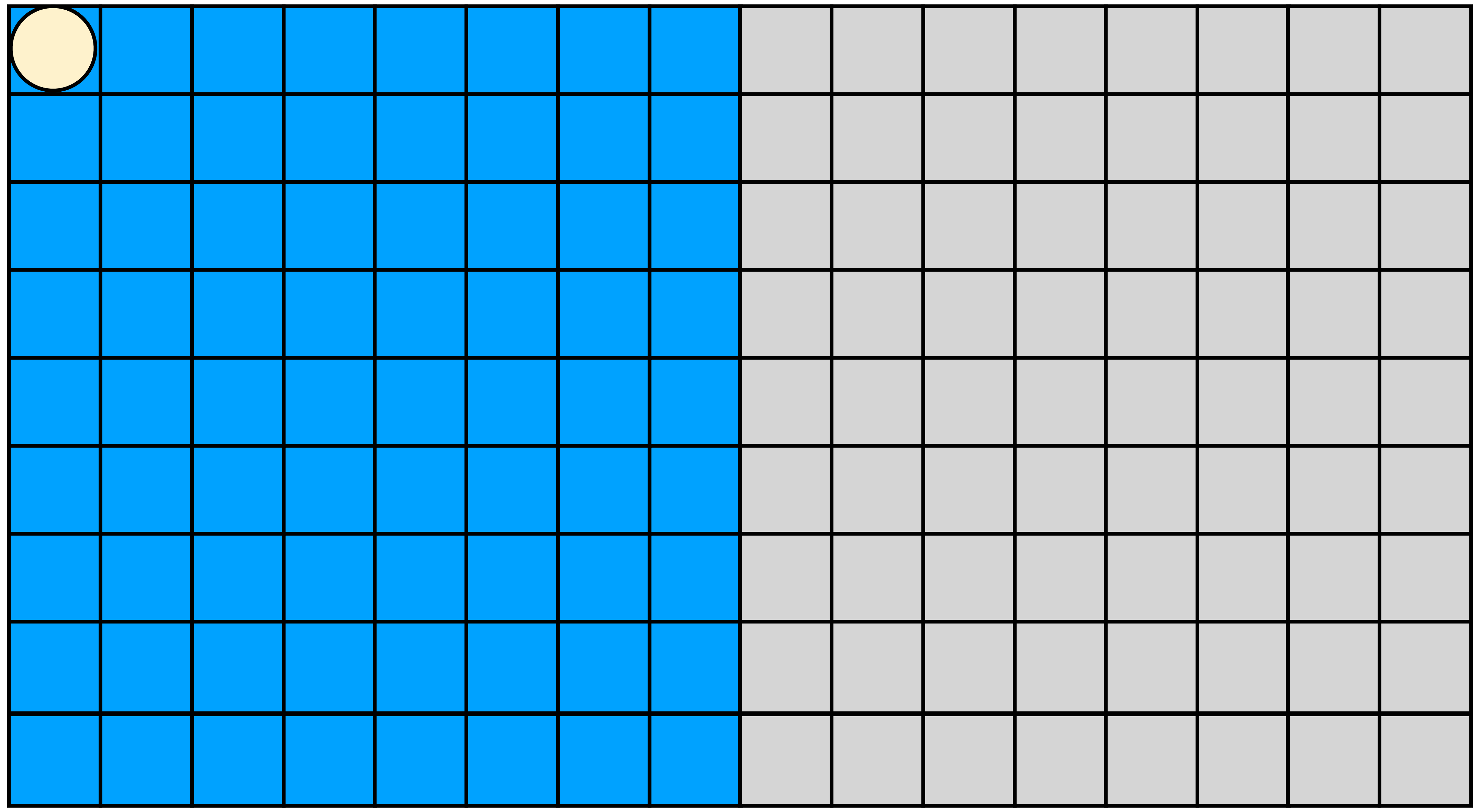
E.g. 8 lines, 2-way associative

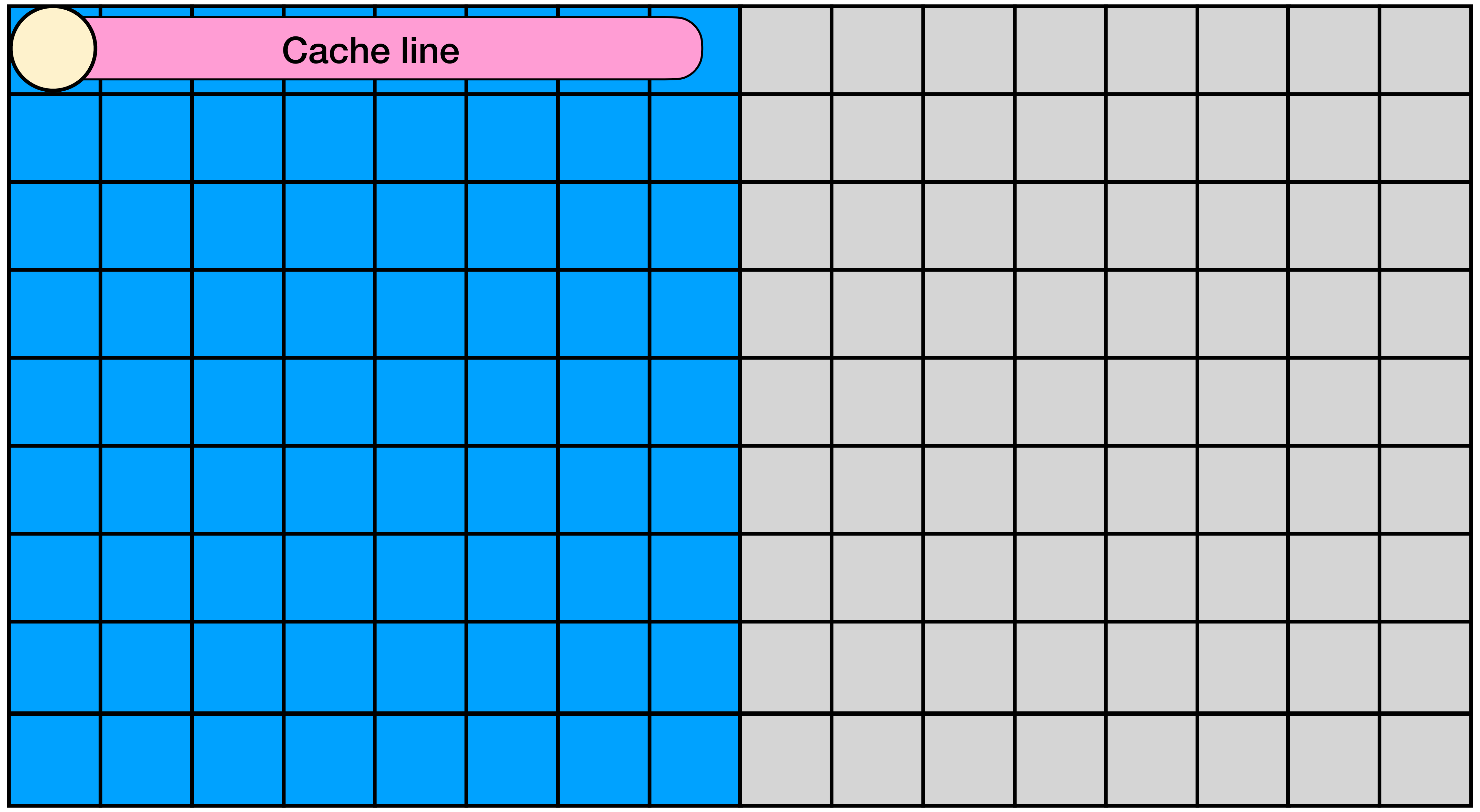
nb of sets = 8 / 2 = 4

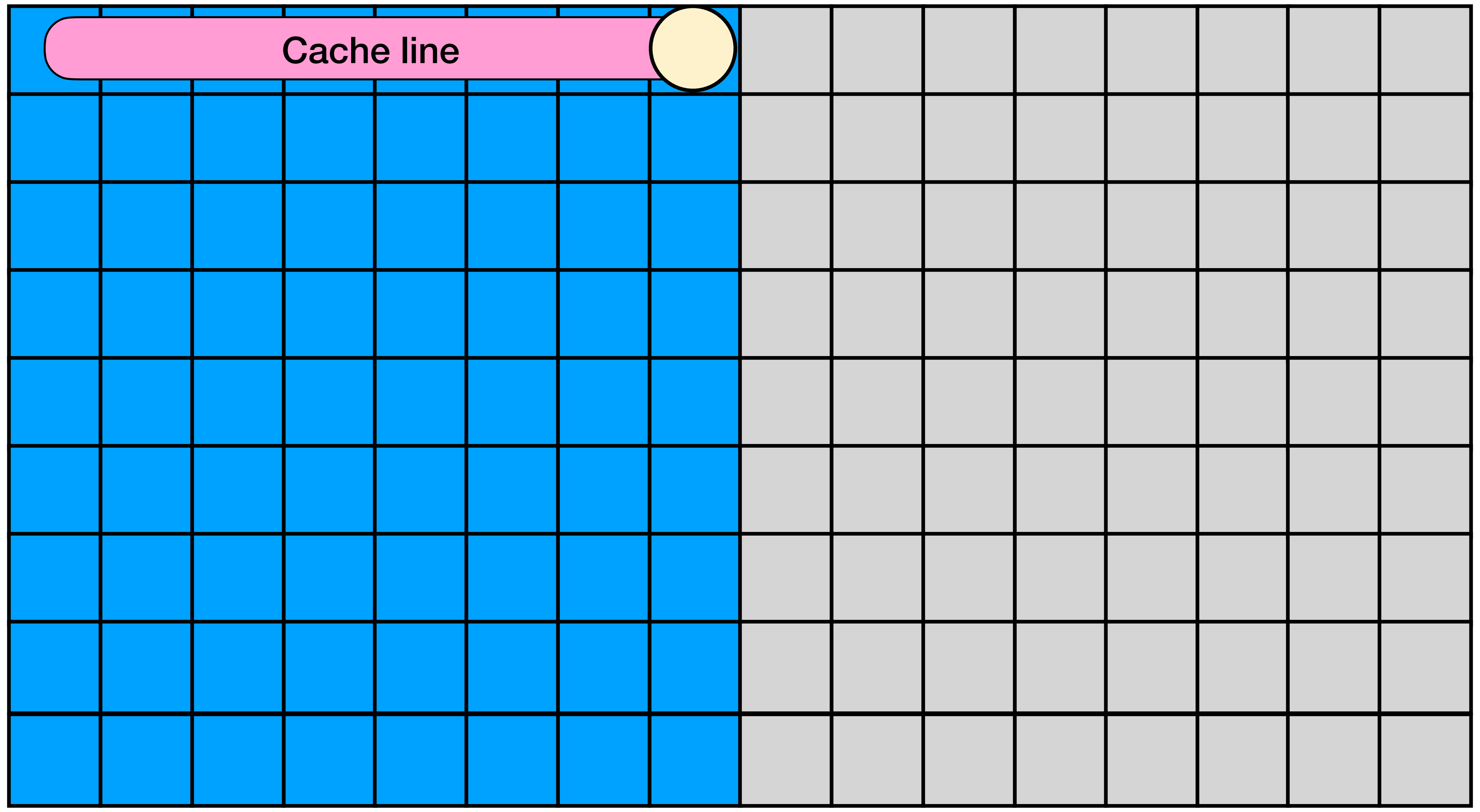
$4 = 2^2$

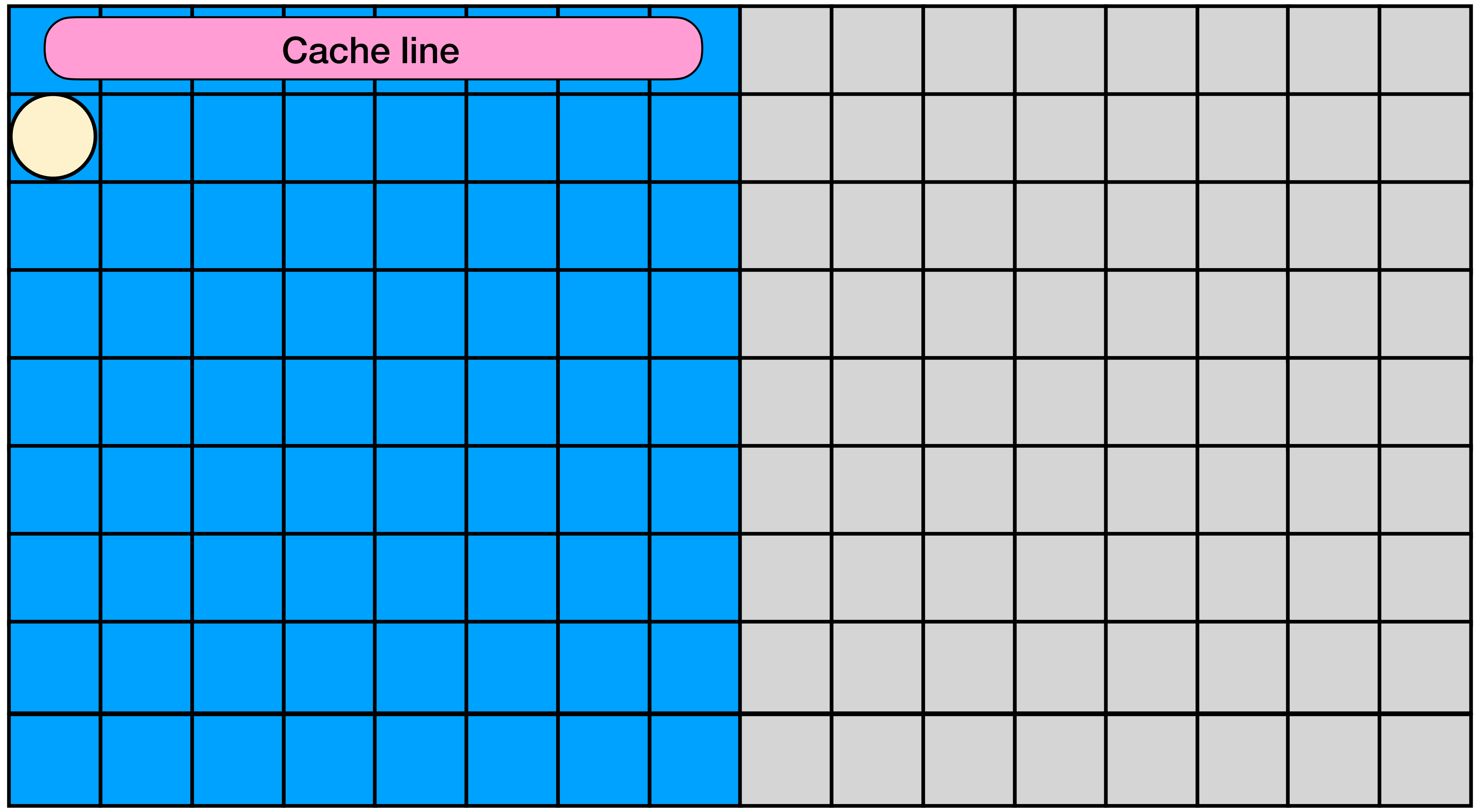
2 represents the **set index** (si)

	Cache	Tag bits
set 0	0000000	000
set 1		
set 2		
set 3		

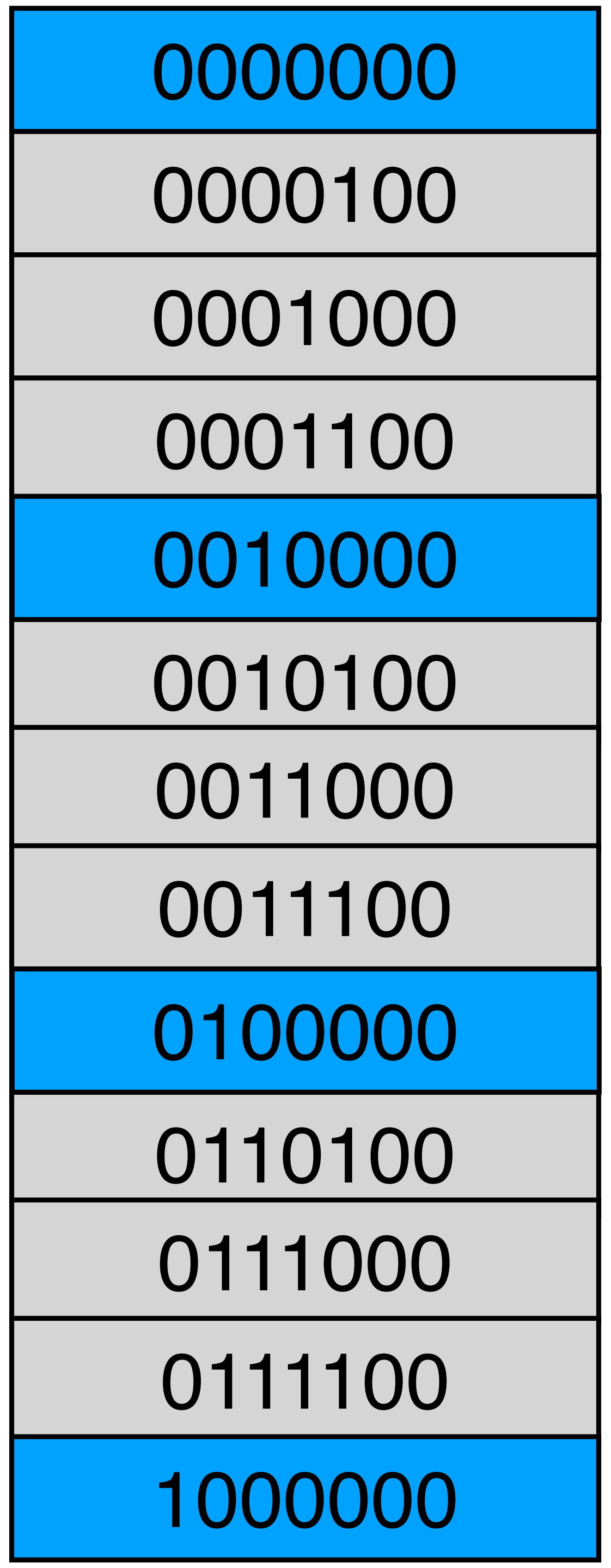



Cache line


Cache line


Cache line

Matrix in memory



E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

A cache is **partitioned** into **sets**

A block can belong to **only one** set

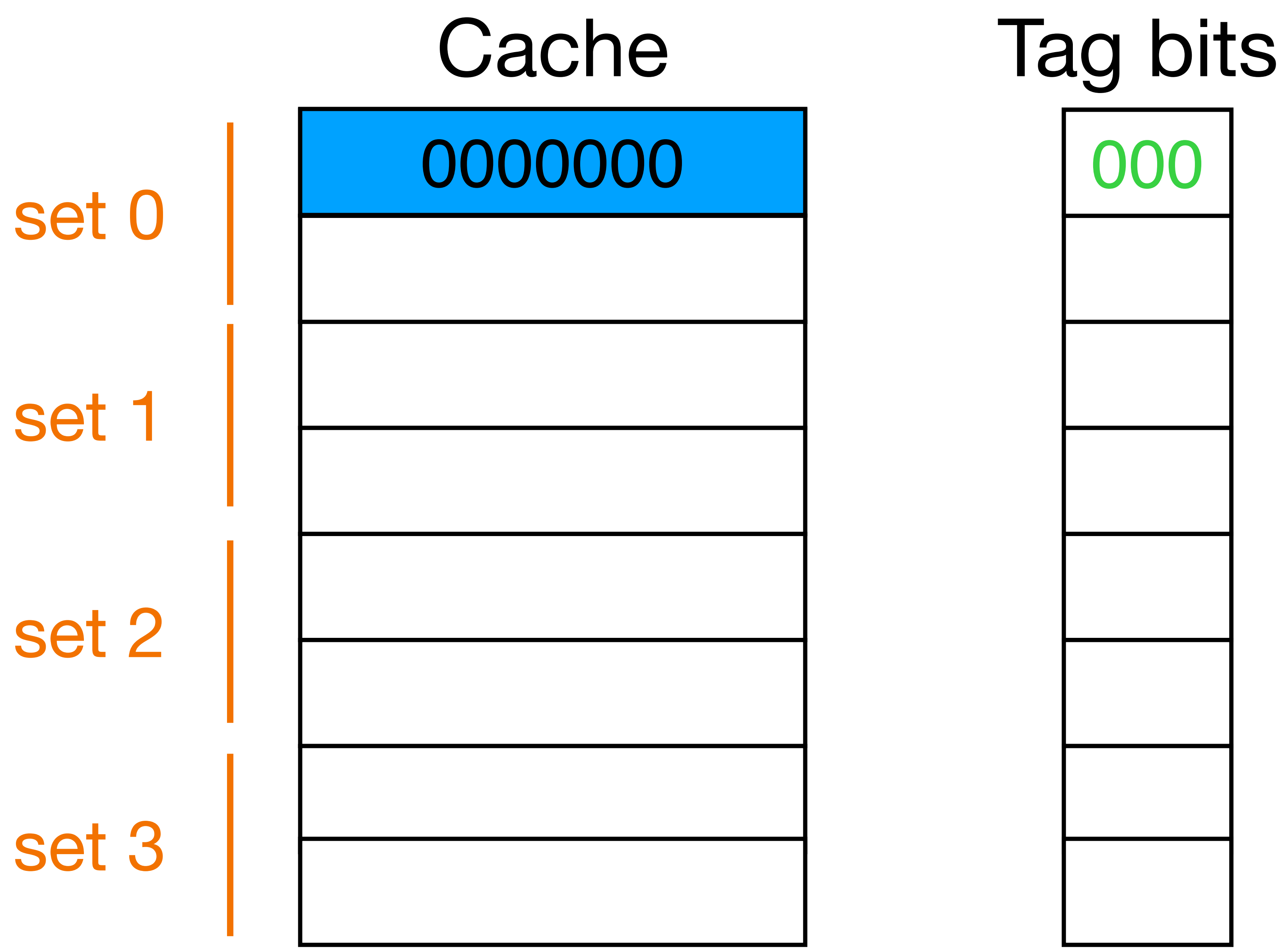
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)



Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

0 0 1 0 0 0 0

tb si bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

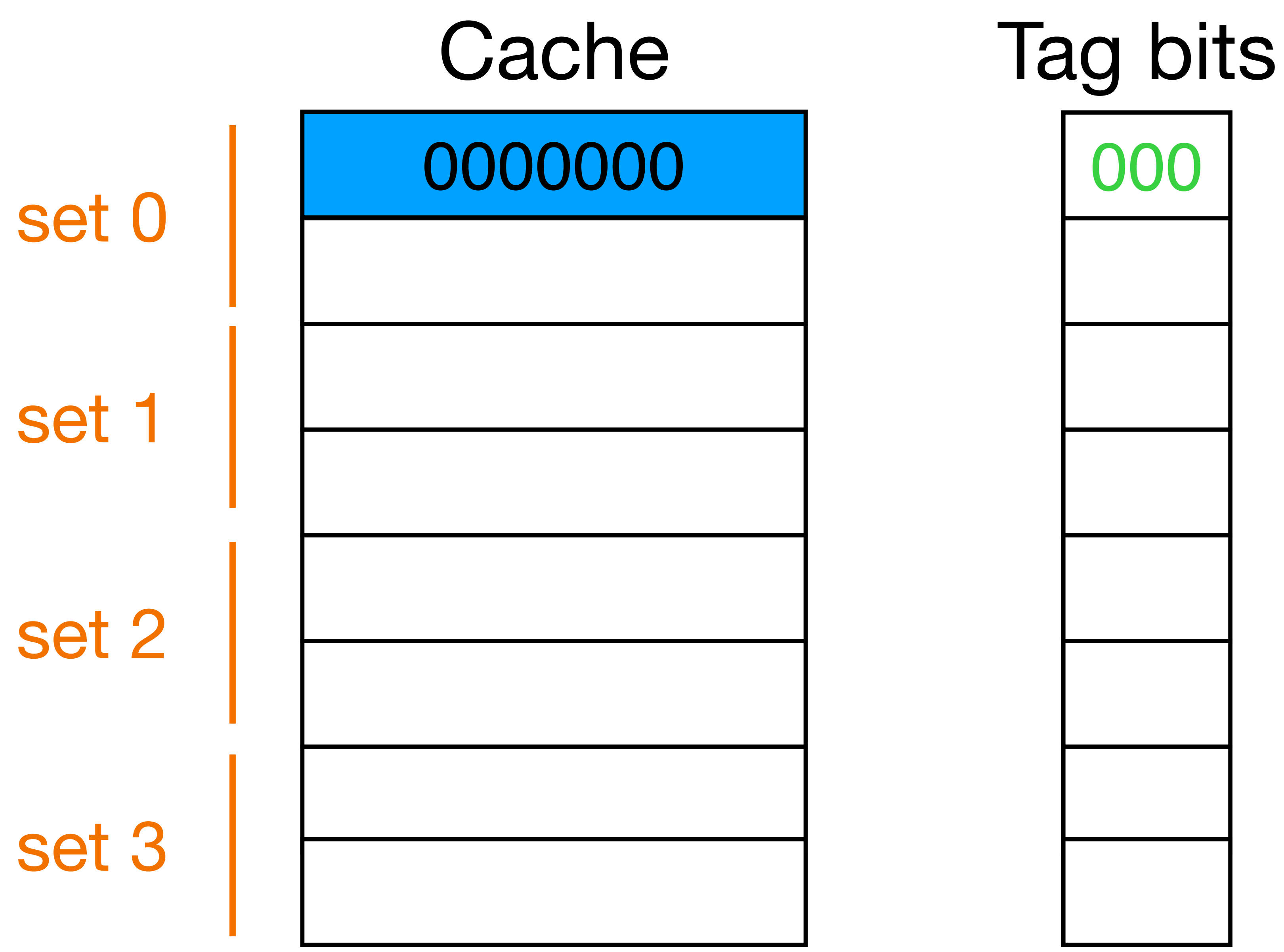
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^{2}$

2 represents the **set index** (si)



Matrix
in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

0 0 1 | 0 0 | 0 0

tb | si | bo

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k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

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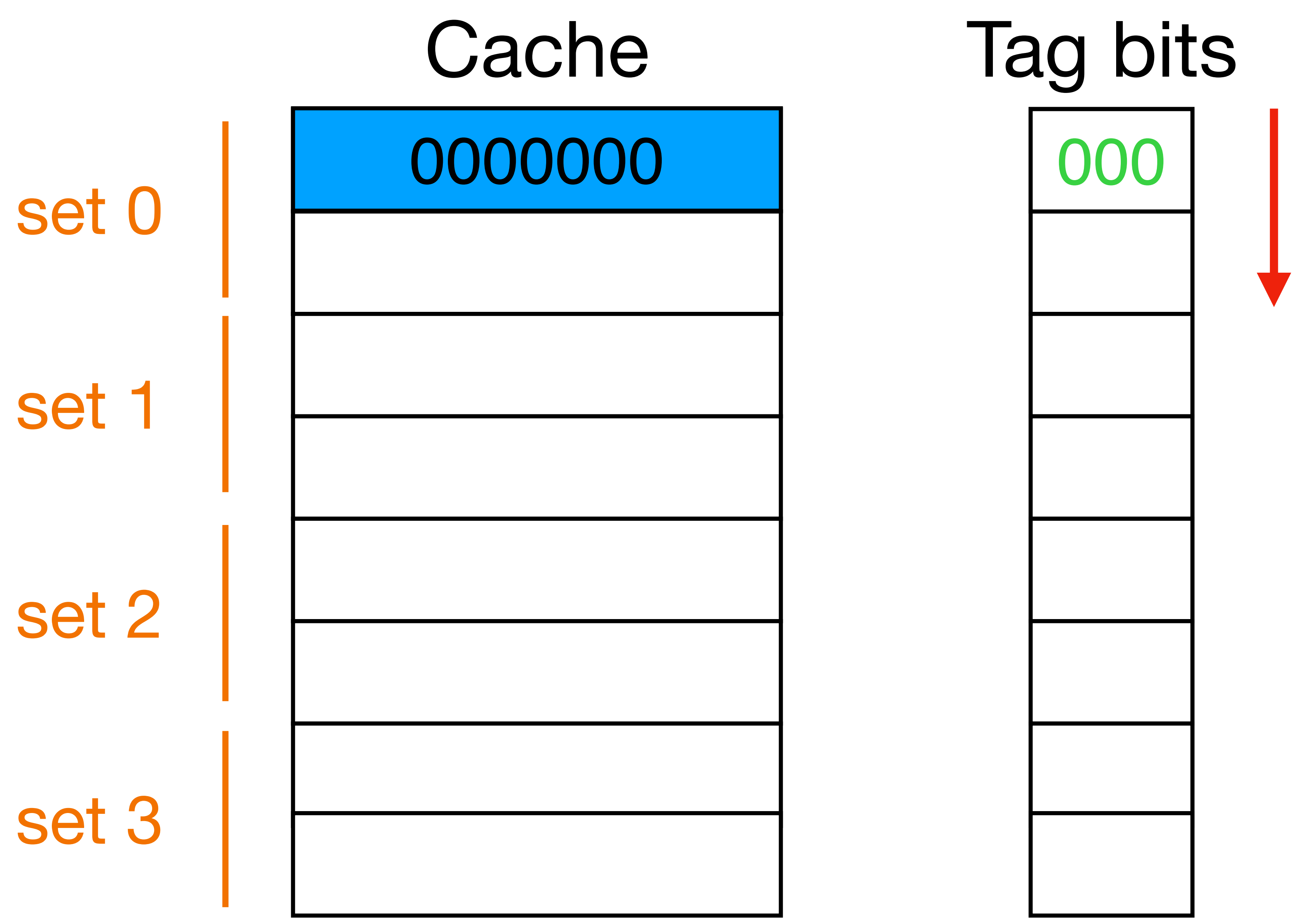


Load

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

0 0 1 | 0 0 | 0 0

tb | si | bo

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)

	Cache	Tag bits
set 0	0000000	000
	0010000	001
set 1		
set 2		
set 3		

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

0 1 0 0 0 0 0

tb si bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

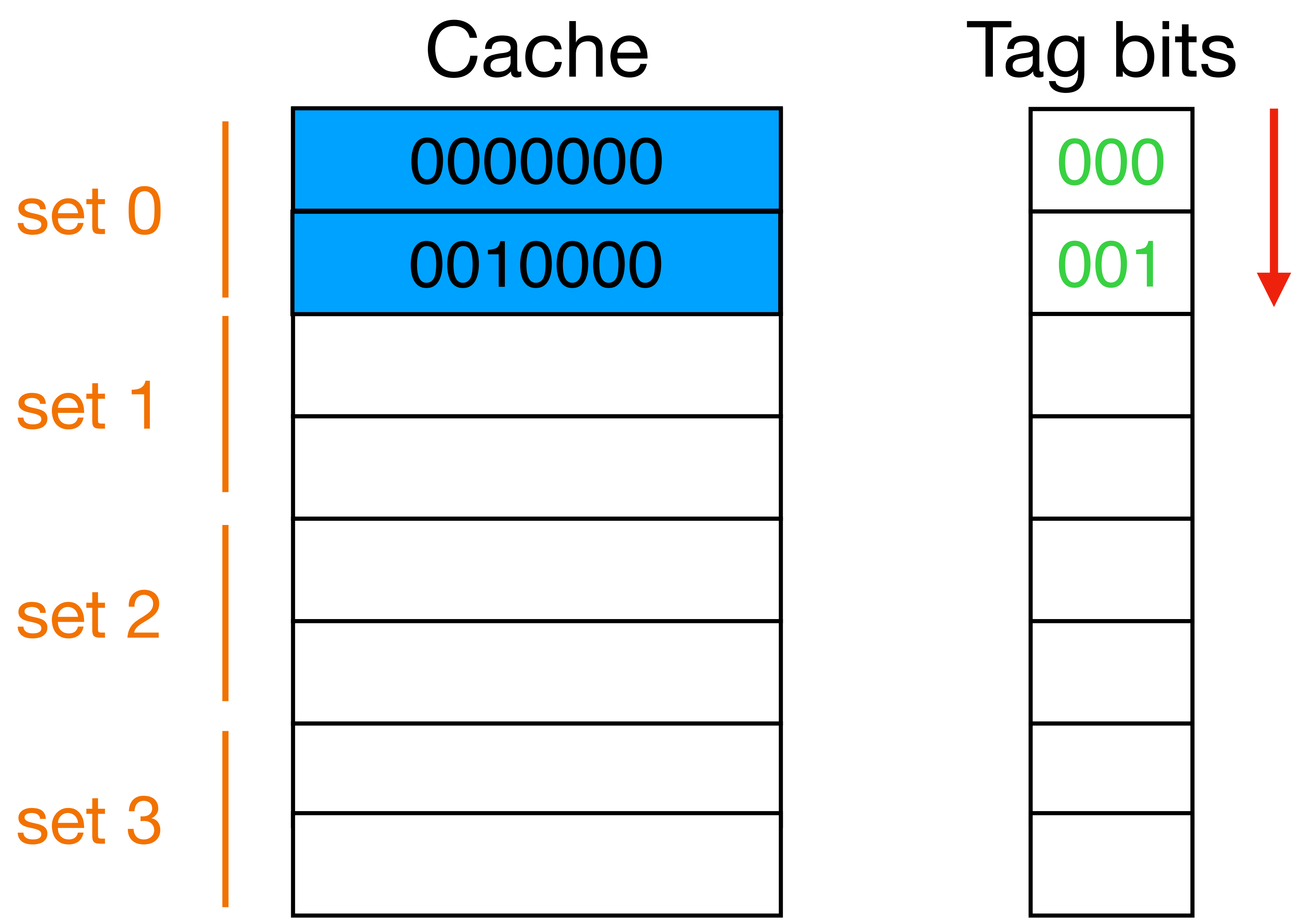
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)



Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

0 1 0 | 0 0 | 0 0

tb | si | bo

A cache is **partitioned** into **sets**

A block can belong to **only one** set

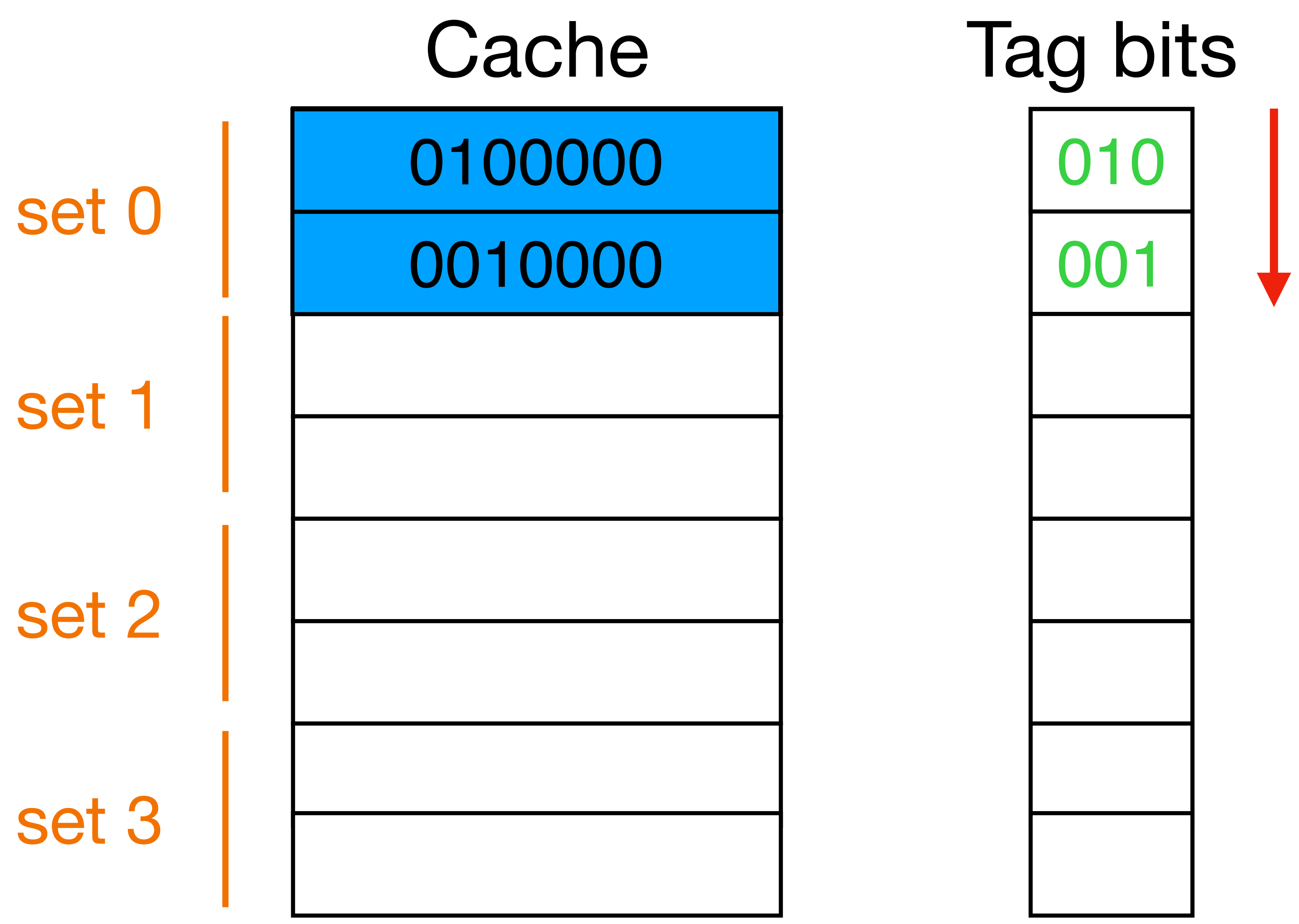
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

$4 = 2^2$

2 represents the **set index** (si)



Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^{2}$

2 represents the **block offset** (bo)

Load

1 0 0 0 0 0 0

tb	si	bo
1 0 0	0 0	0 0

A cache is **partitioned** into **sets**

A block can belong to **only one** set

k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

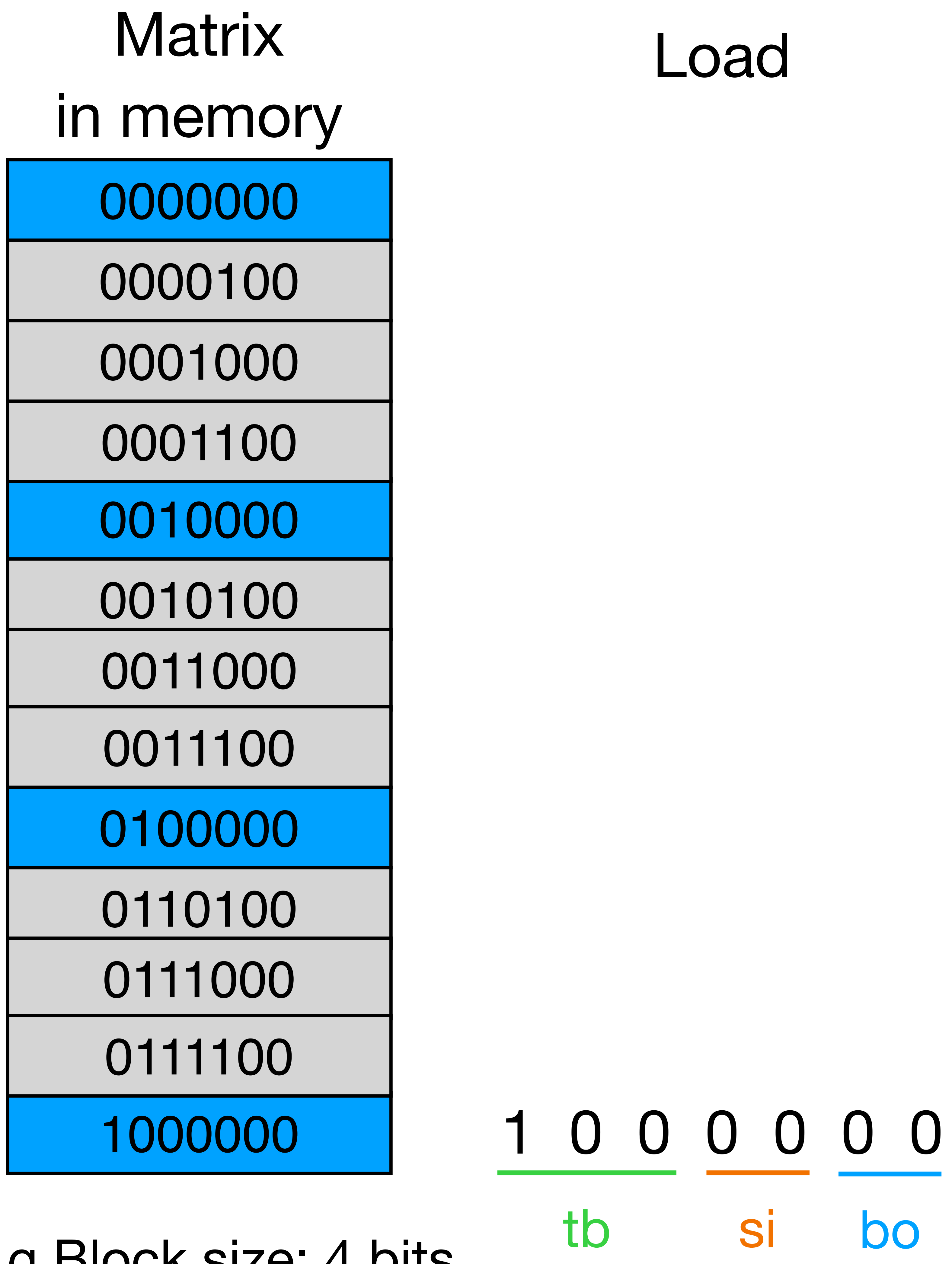
nb of sets = 8 / 2 = 4

$4 = 2^{2}$

2 represents the **set index** (si)

	Cache	Tag bits
set 0	0100000	010
	0010000	001
set 1		
set 2		
set 3		

Load



E.g Block size: 4 bits

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2 represents the

block offset (bo)

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nb of sets = 8 / 2 = 4

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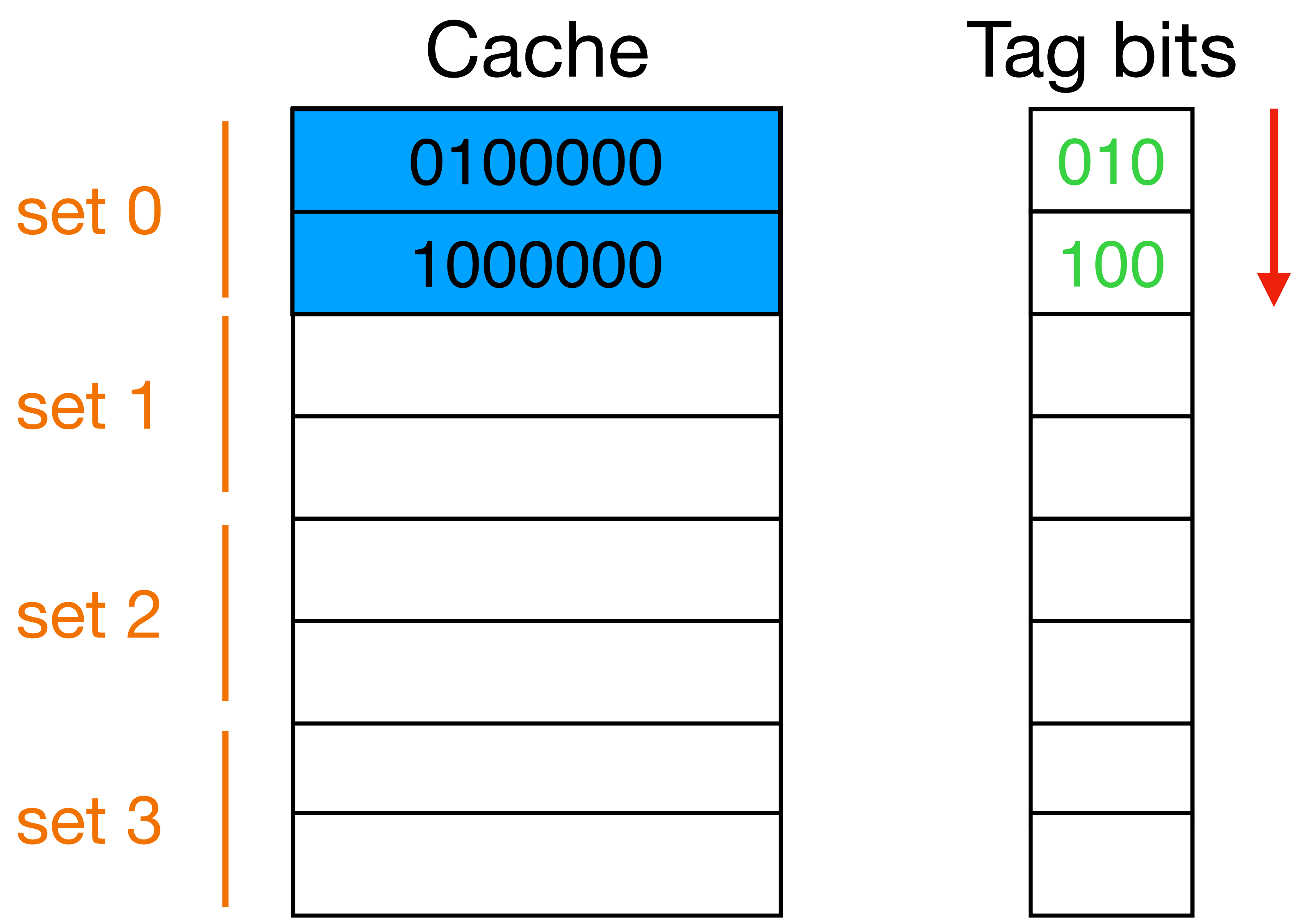

Matrix in memory

0000000
0000100
0001000
0001100
0010000
0010100
0011000
0011100
0100000
0110100
0111000
0111100
1000000

E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

0 0 0 | 0 0 | 0 0

tb | si | bo

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A block can belong to **only one** set

k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

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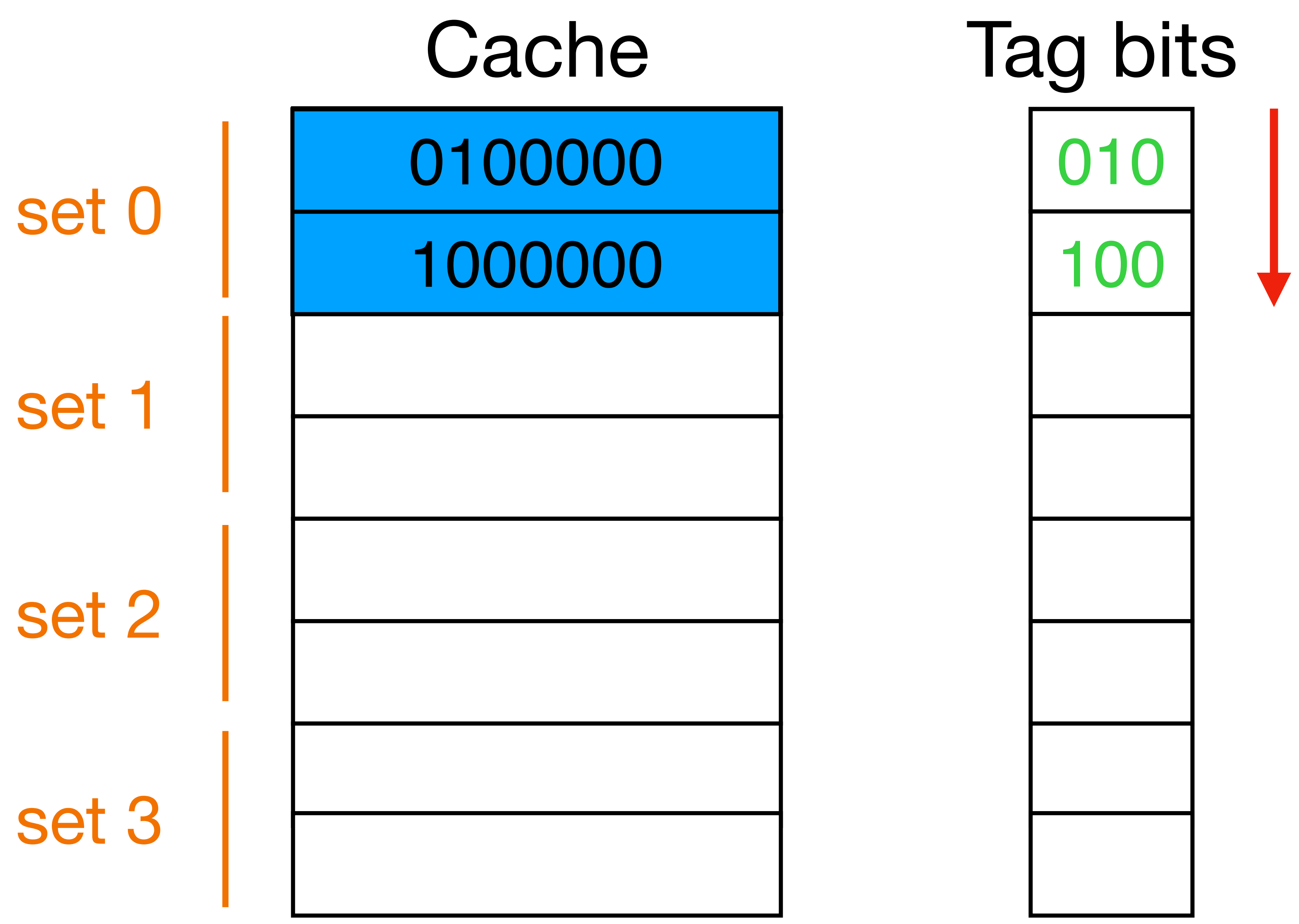
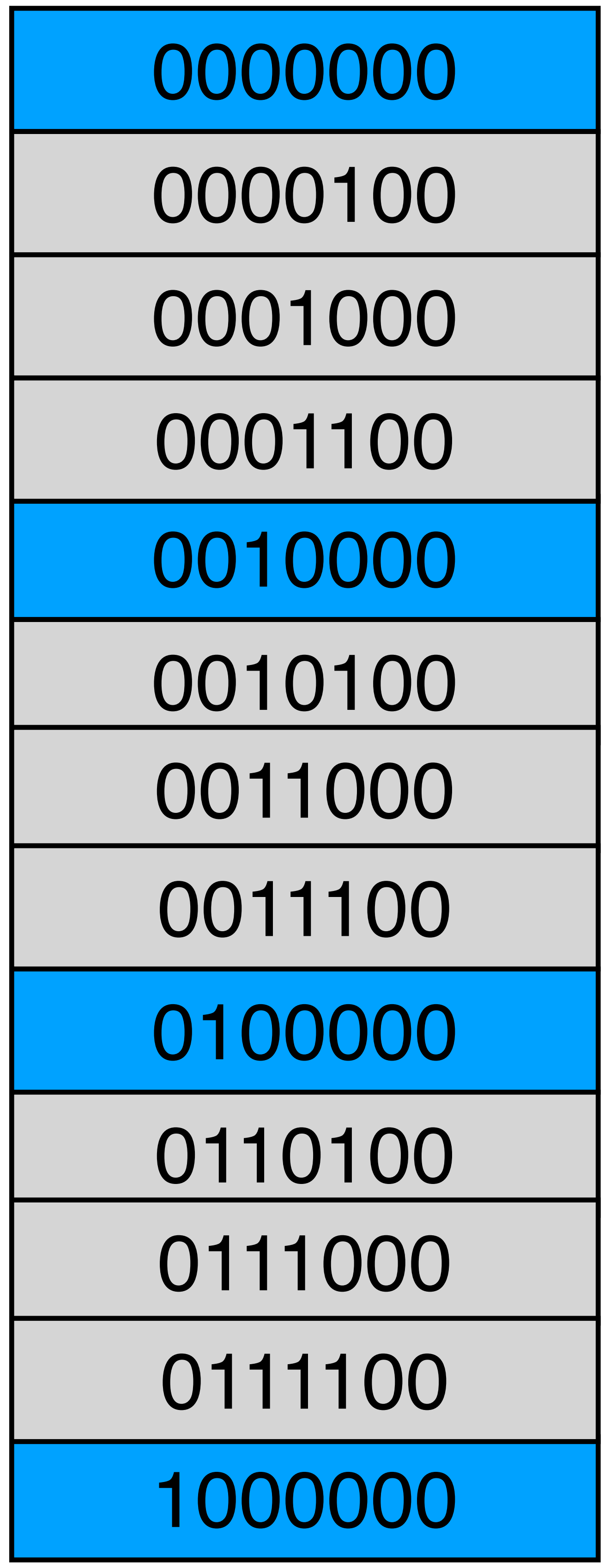


Matrix in memory



E.g Block size: 4 bits

$4 = 2^2$

2 represents the **block offset** (bo)

Load

A cache is **partitioned** into **sets**

A block can belong to **only one** set

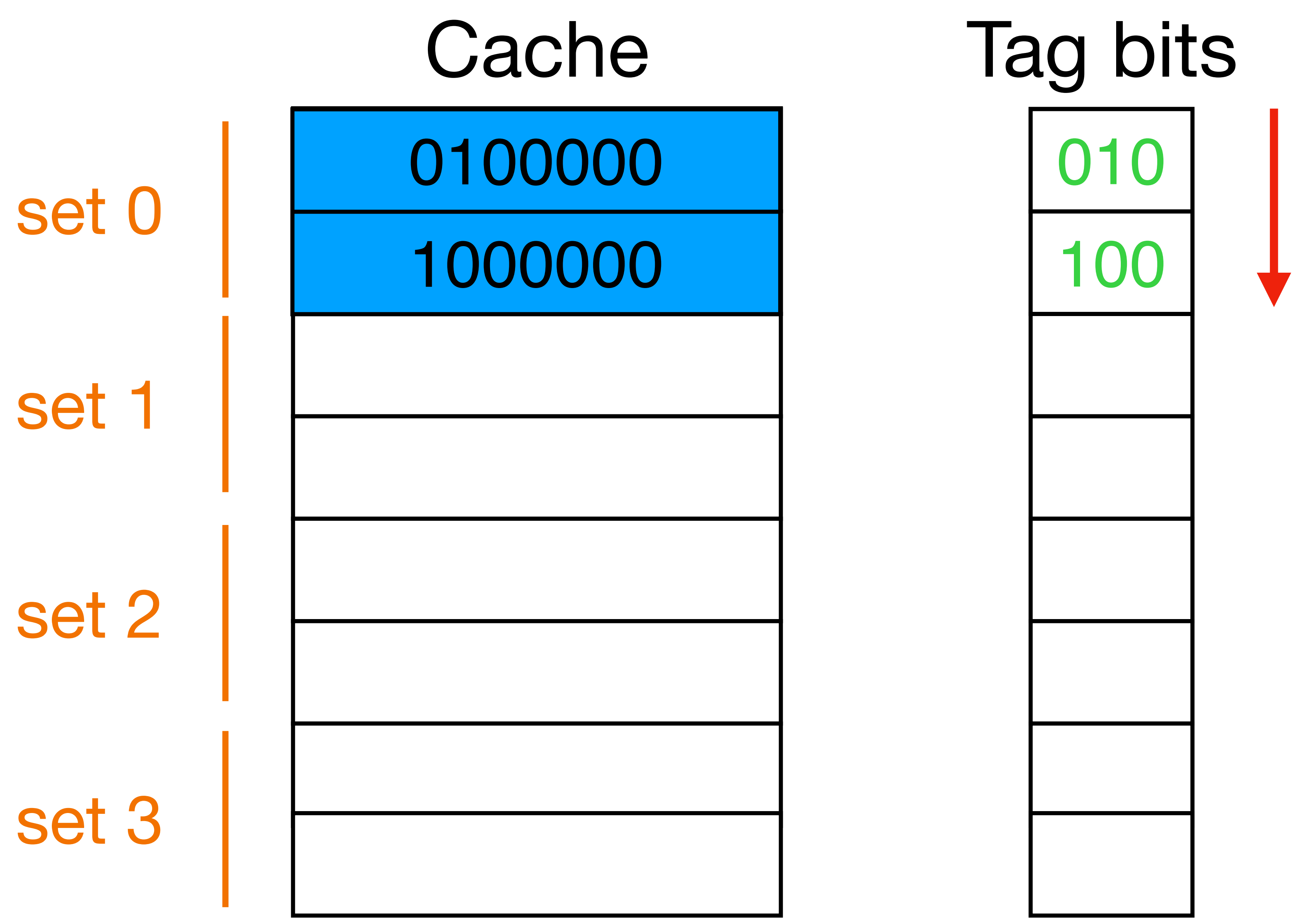
k-way associative cache: k lines per set

E.g. 8 lines, 2-way associative

nb of sets = 8 / 2 = 4

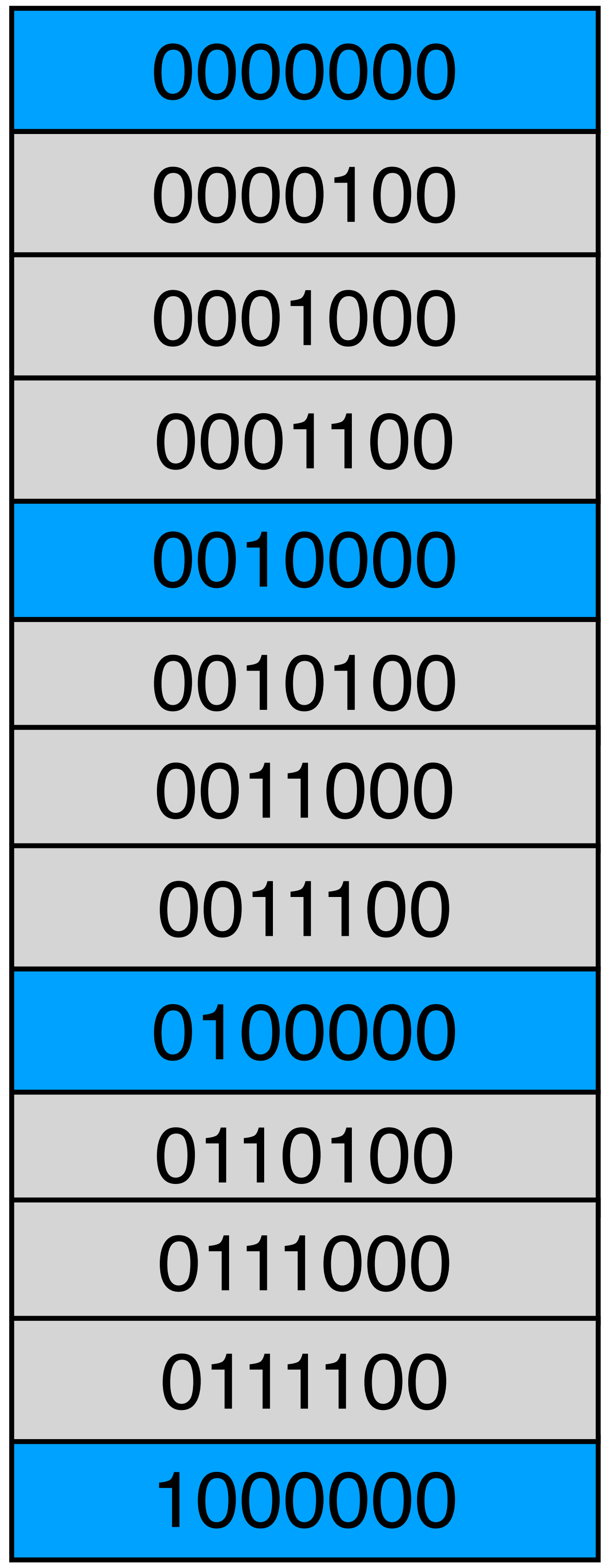
$4 = 2^2$

2 represents the **set index** (si)



The distribution is not even, we used **only one set**

Matrix in memory



E.g Block size: 4 bits

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2 represents the **block offset** (bo)

Load

0 0 0 0 0 0 0

tb si bo

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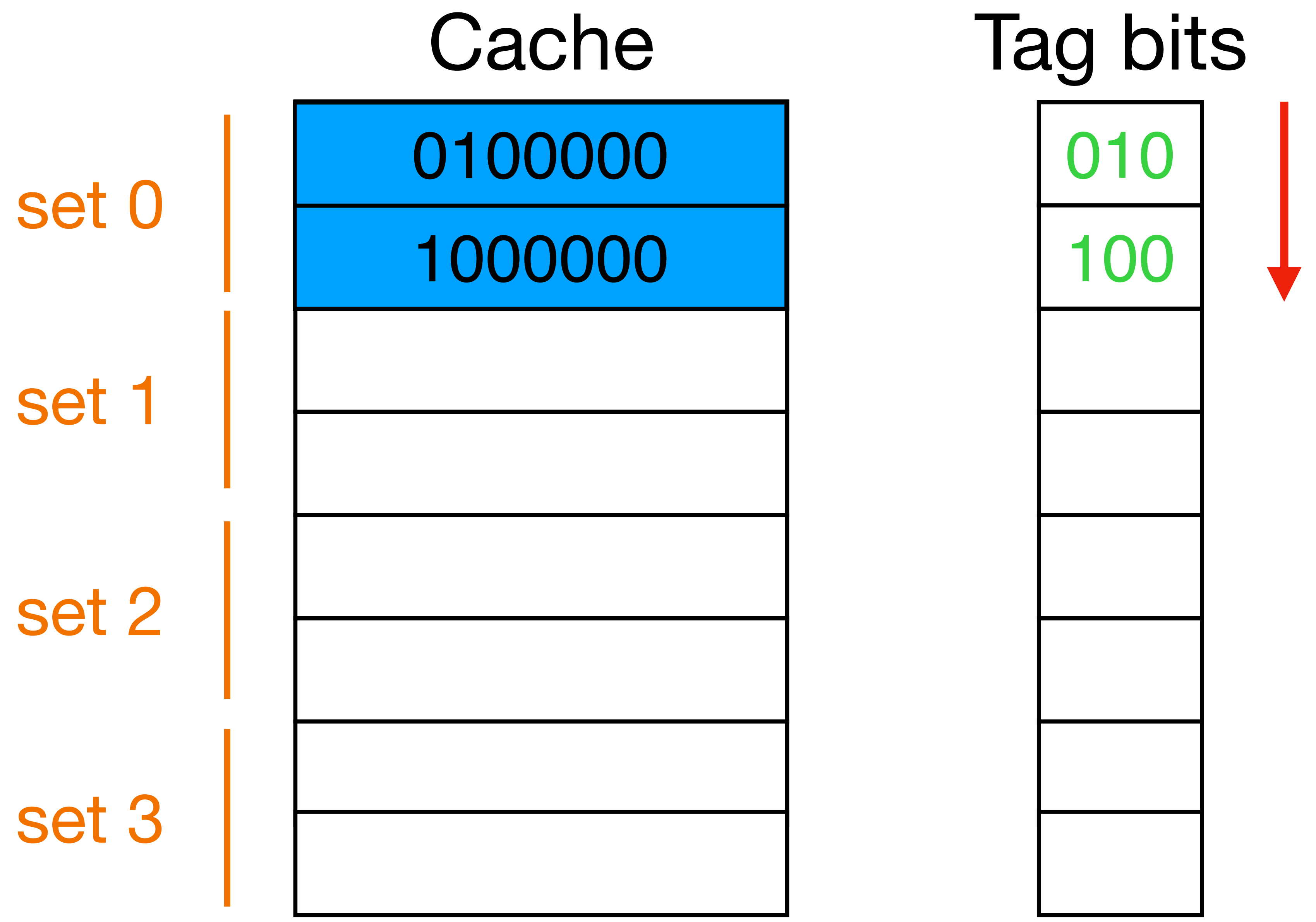

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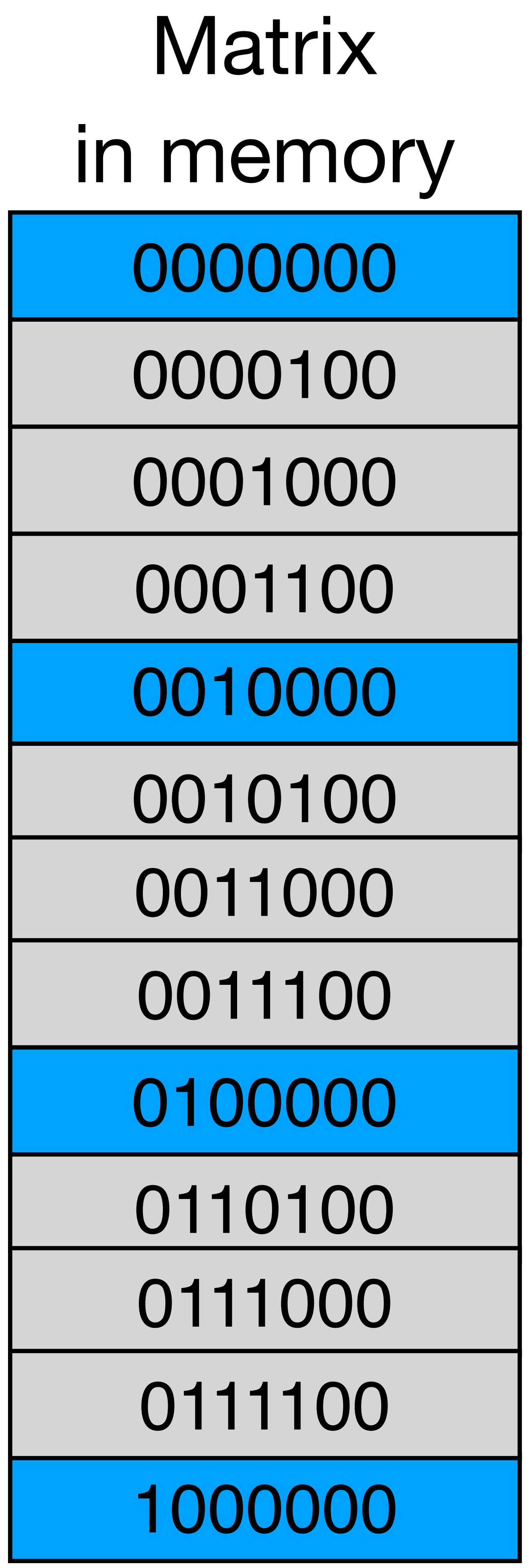

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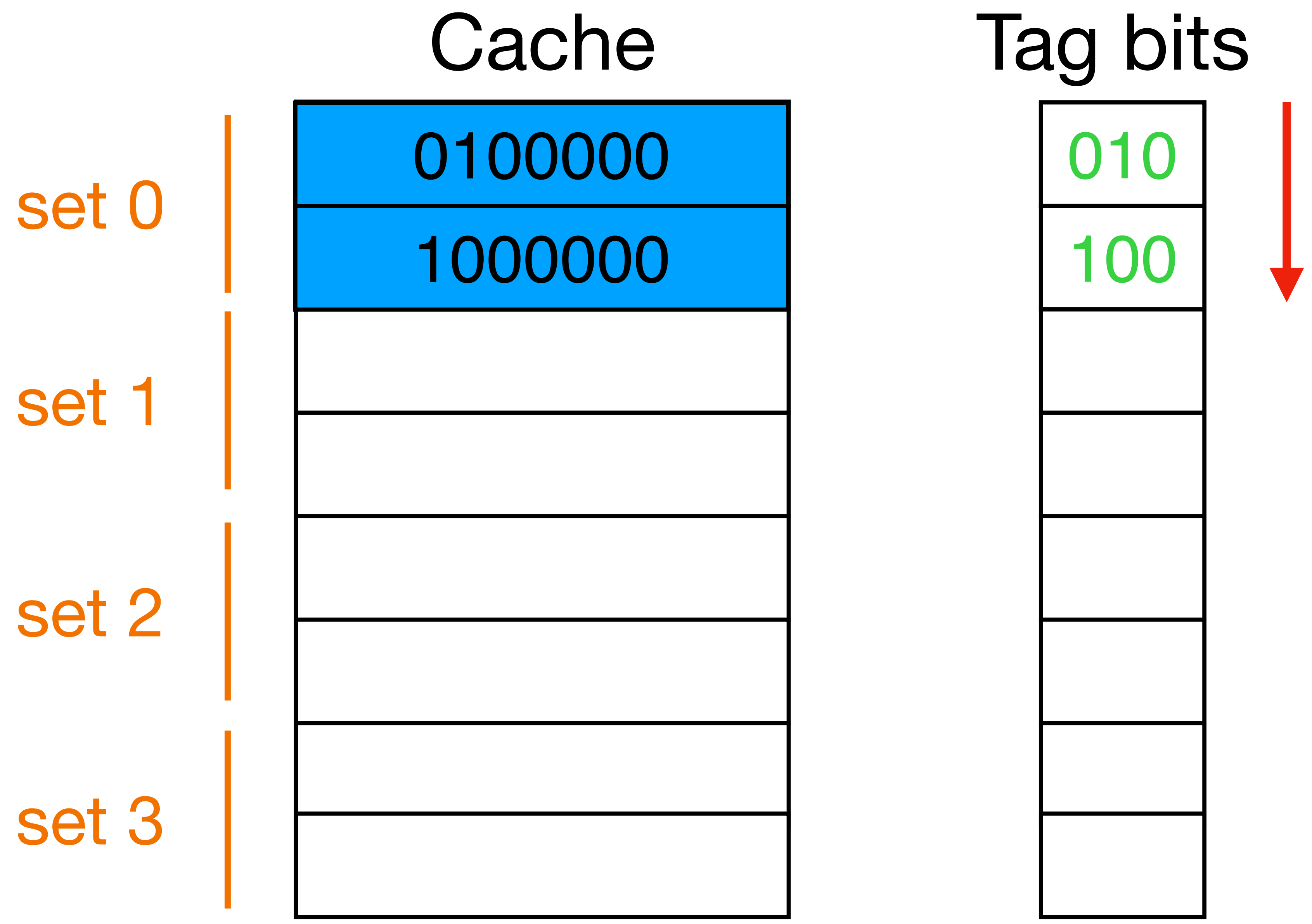

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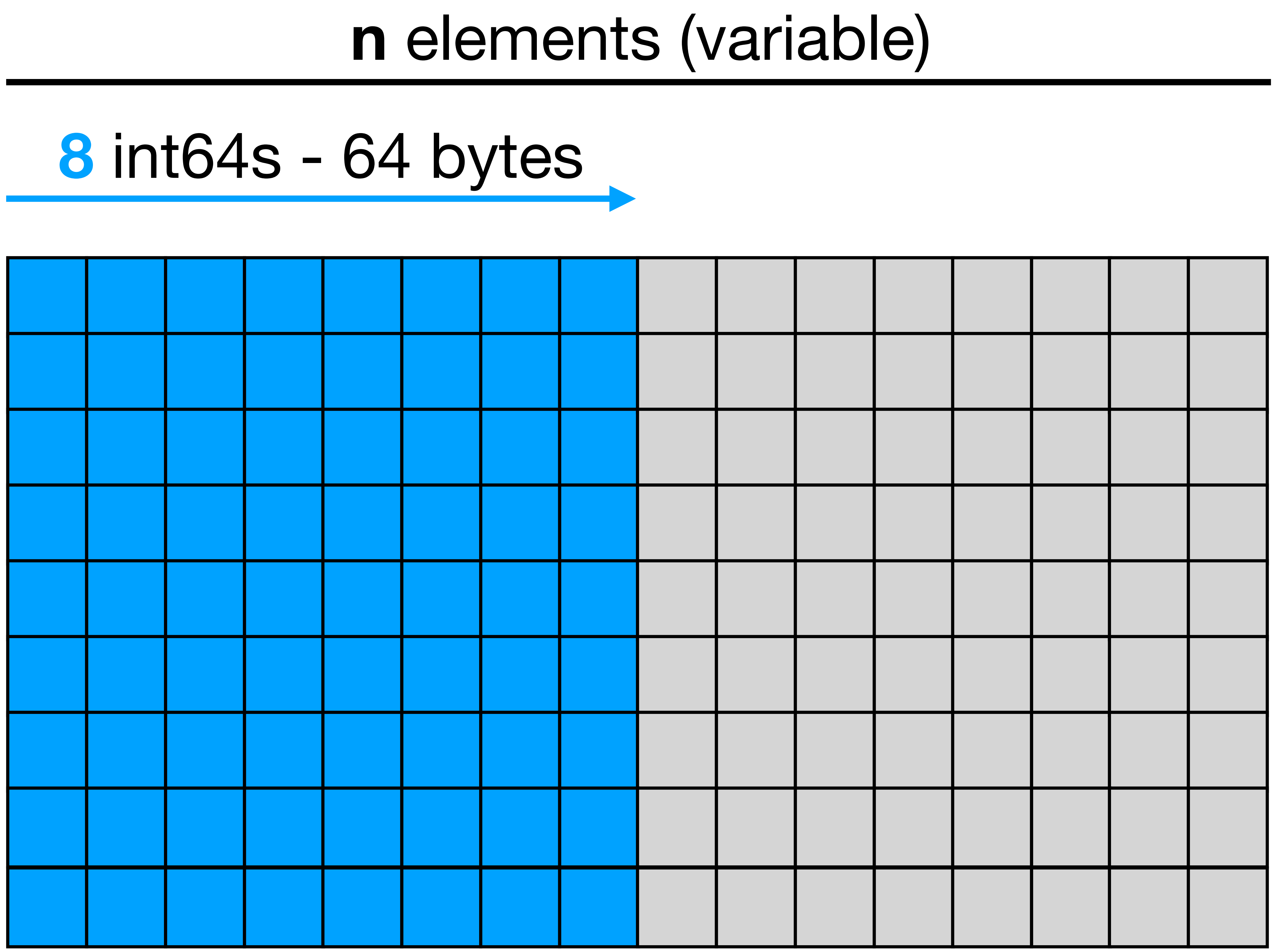
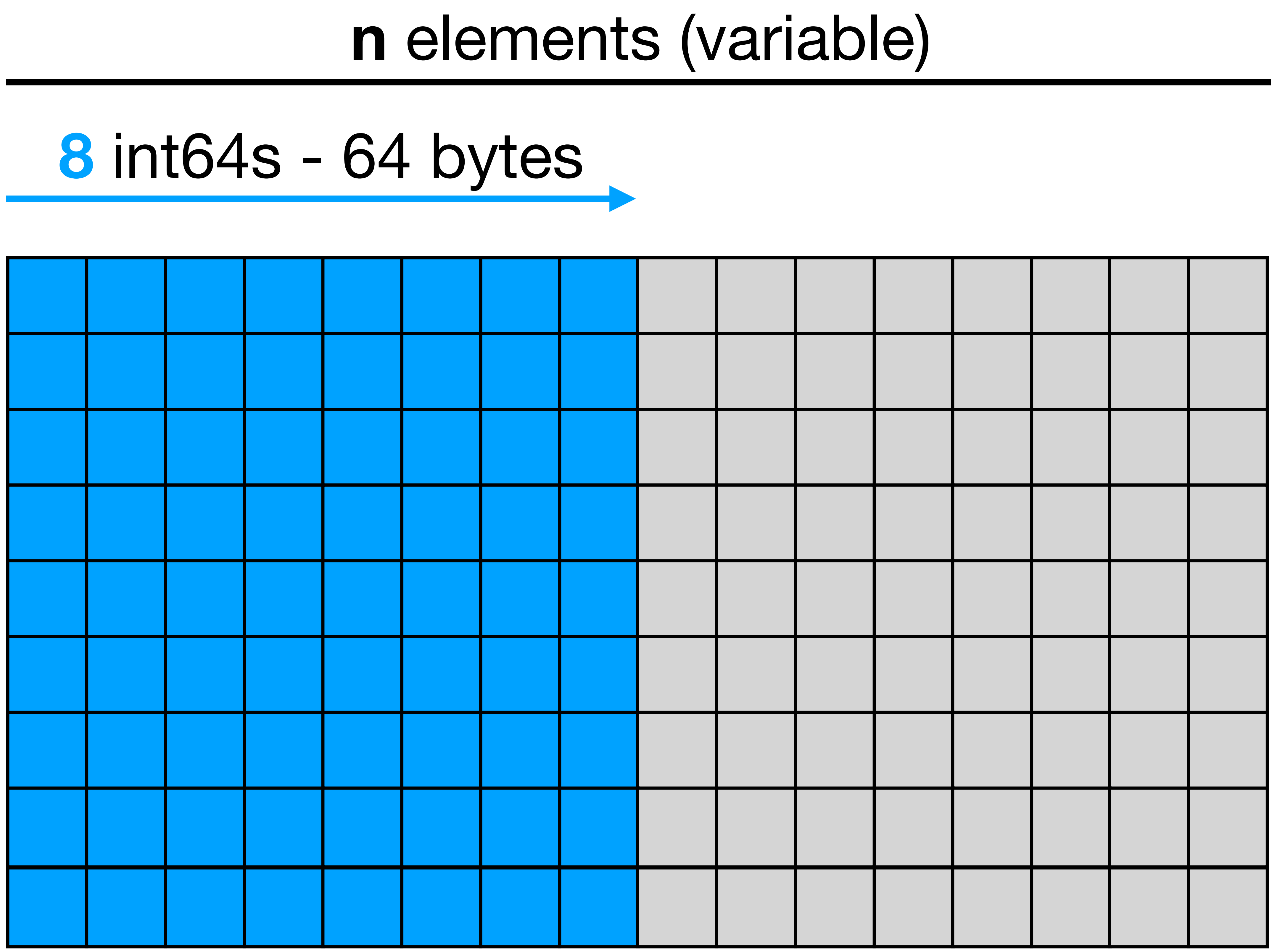
It will generate a lot of cache misses (conflict miss)

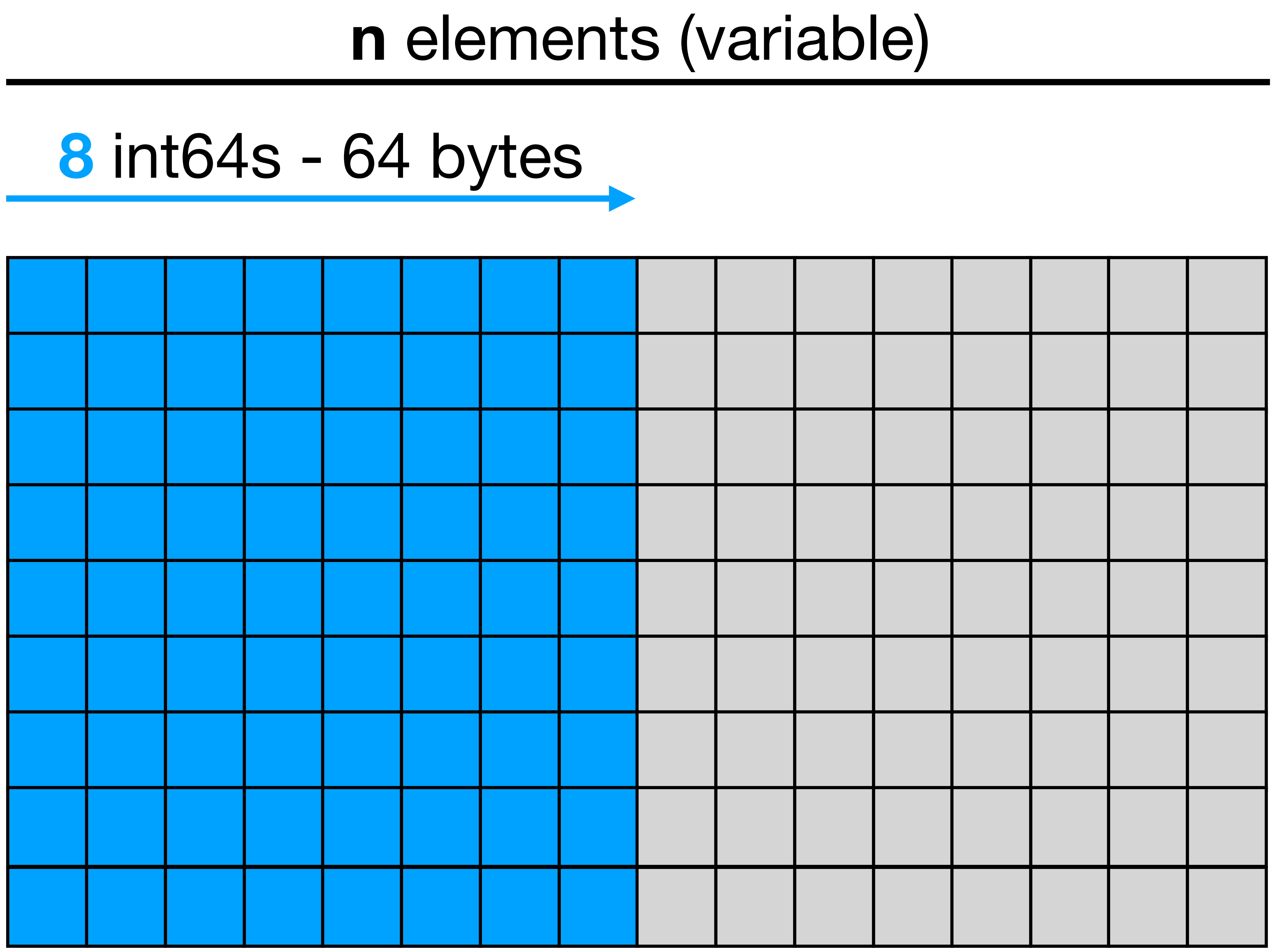
This constant stride is called the **critical stride**


n elements (variable)
8 int64s - 64 bytes

- Critical stride = nb sets x cache line size



- Critical stride = nb sets x cache line size
- Example with an Intel Core i5-7300:
  - Cache line = 64 bytes
  - 32 KB, 8-way set associative, **64 sets**
  - Critical stride = 64 x 64 = **4 KB**



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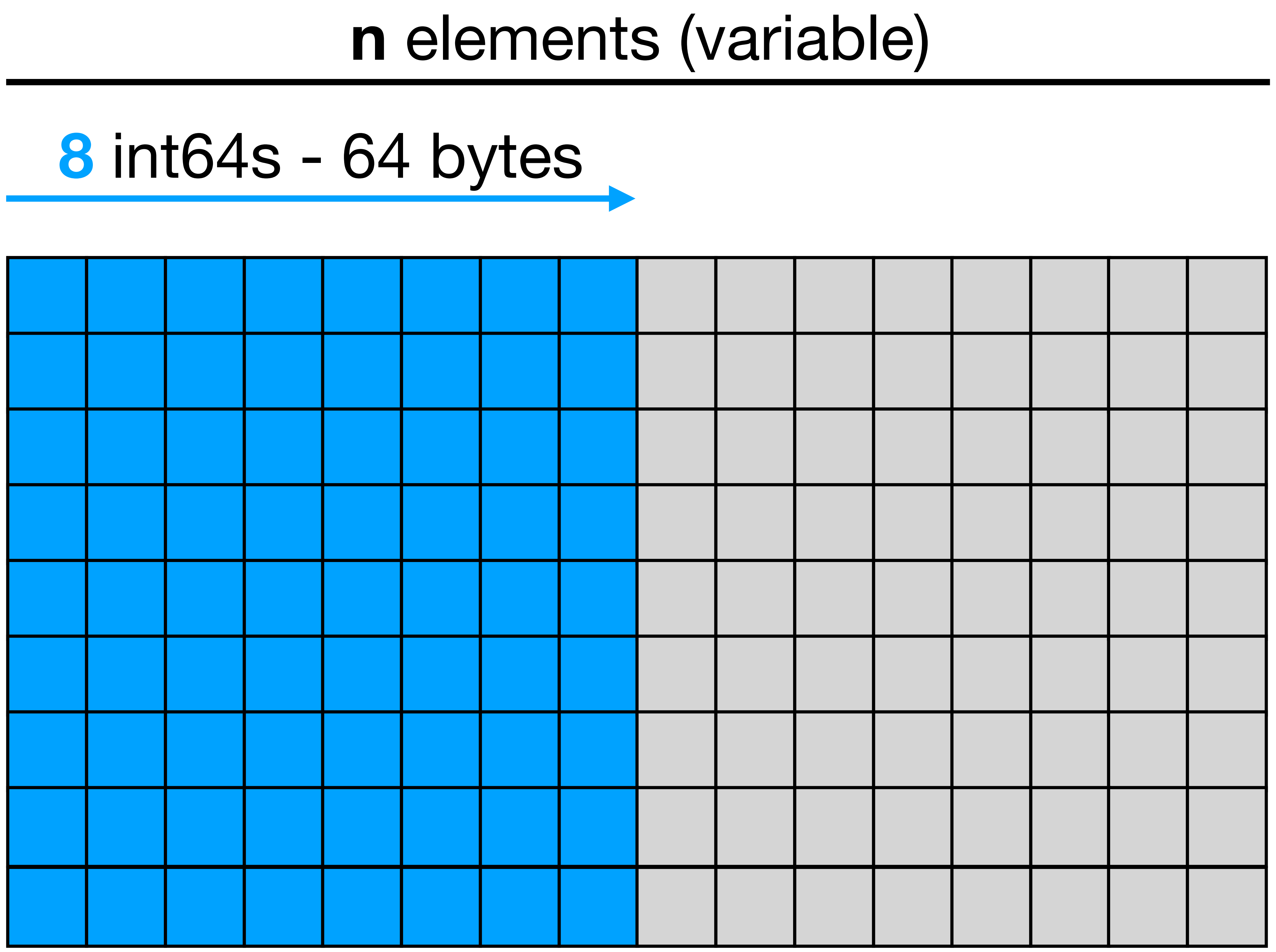

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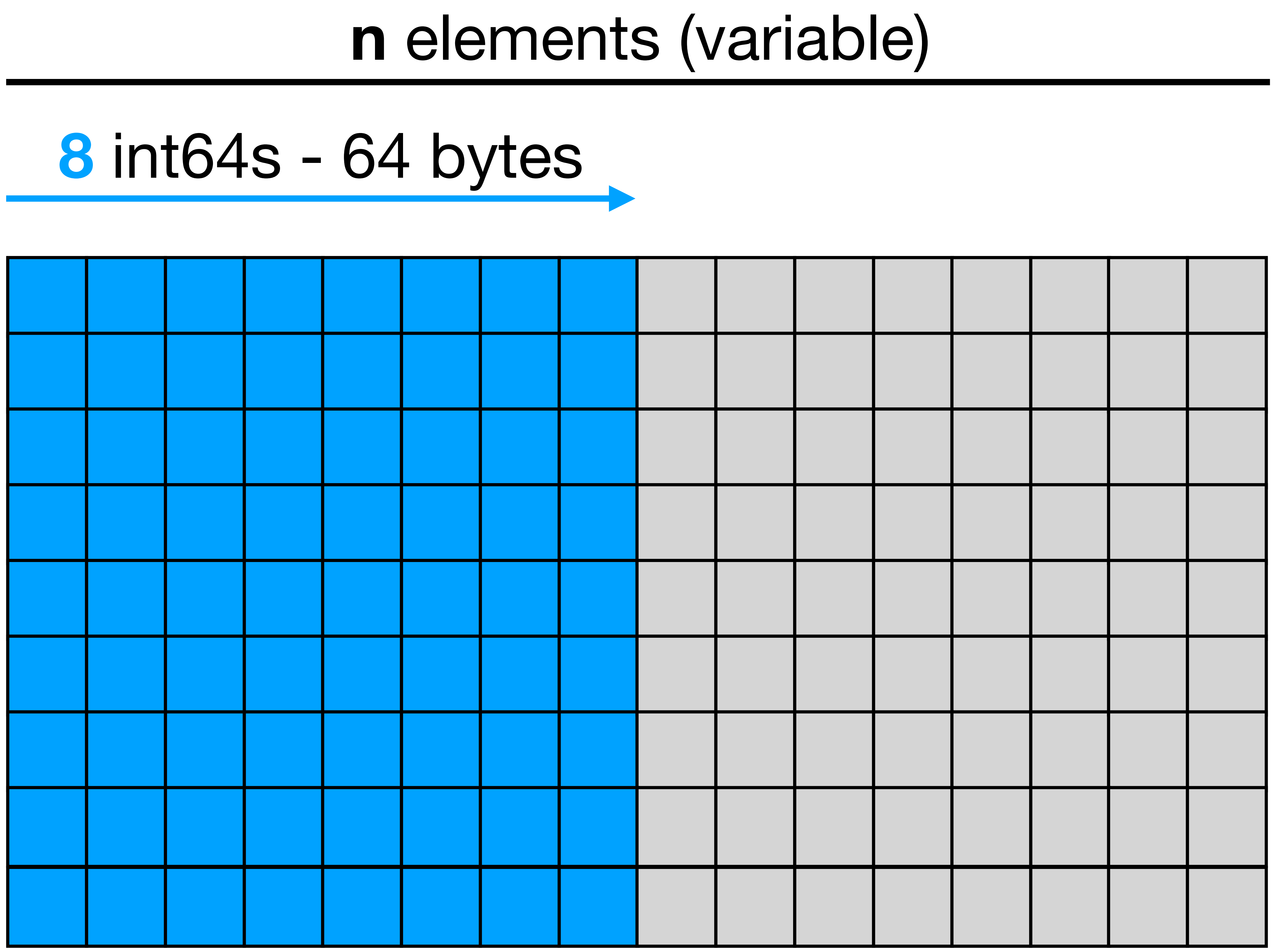

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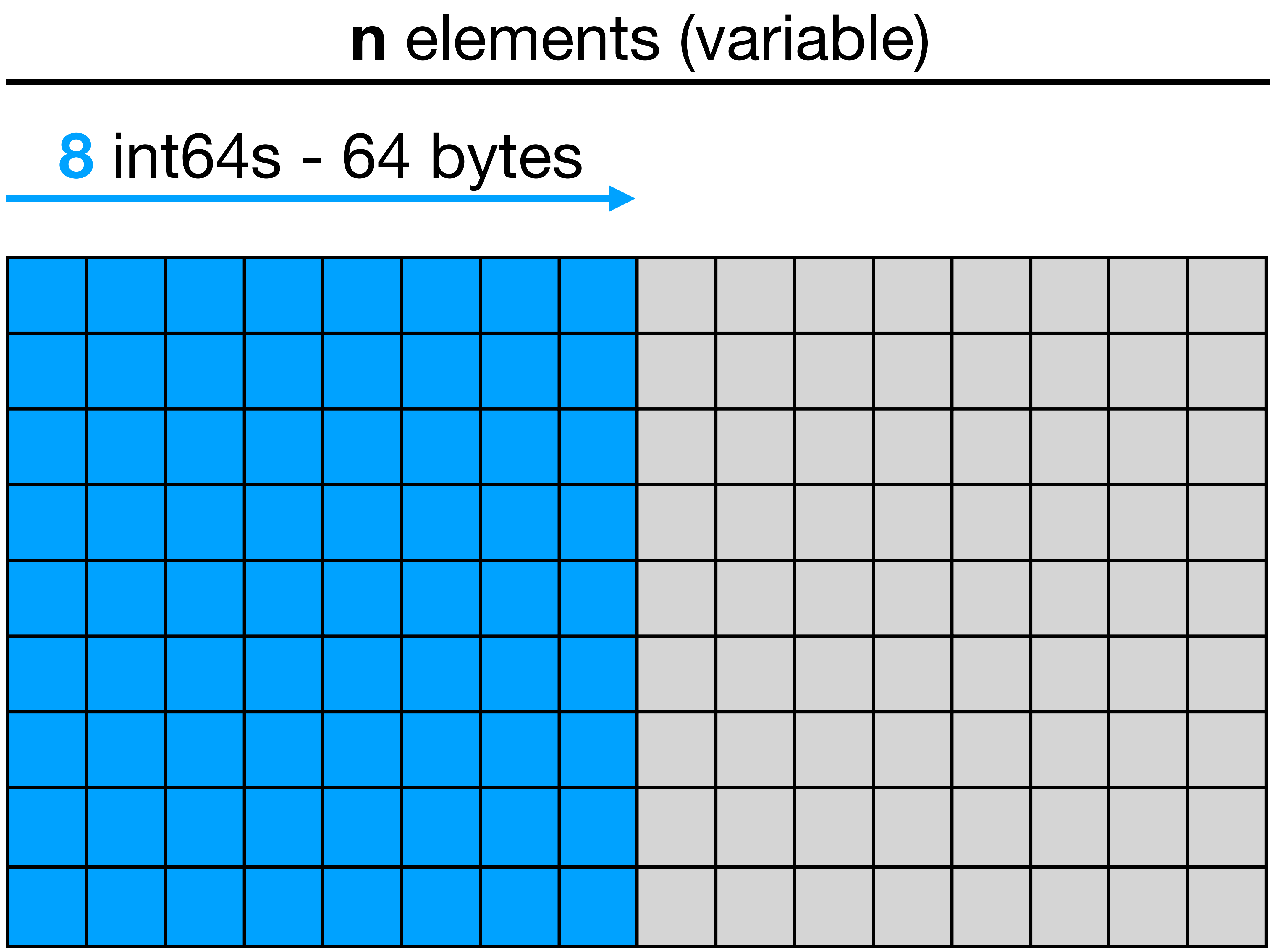

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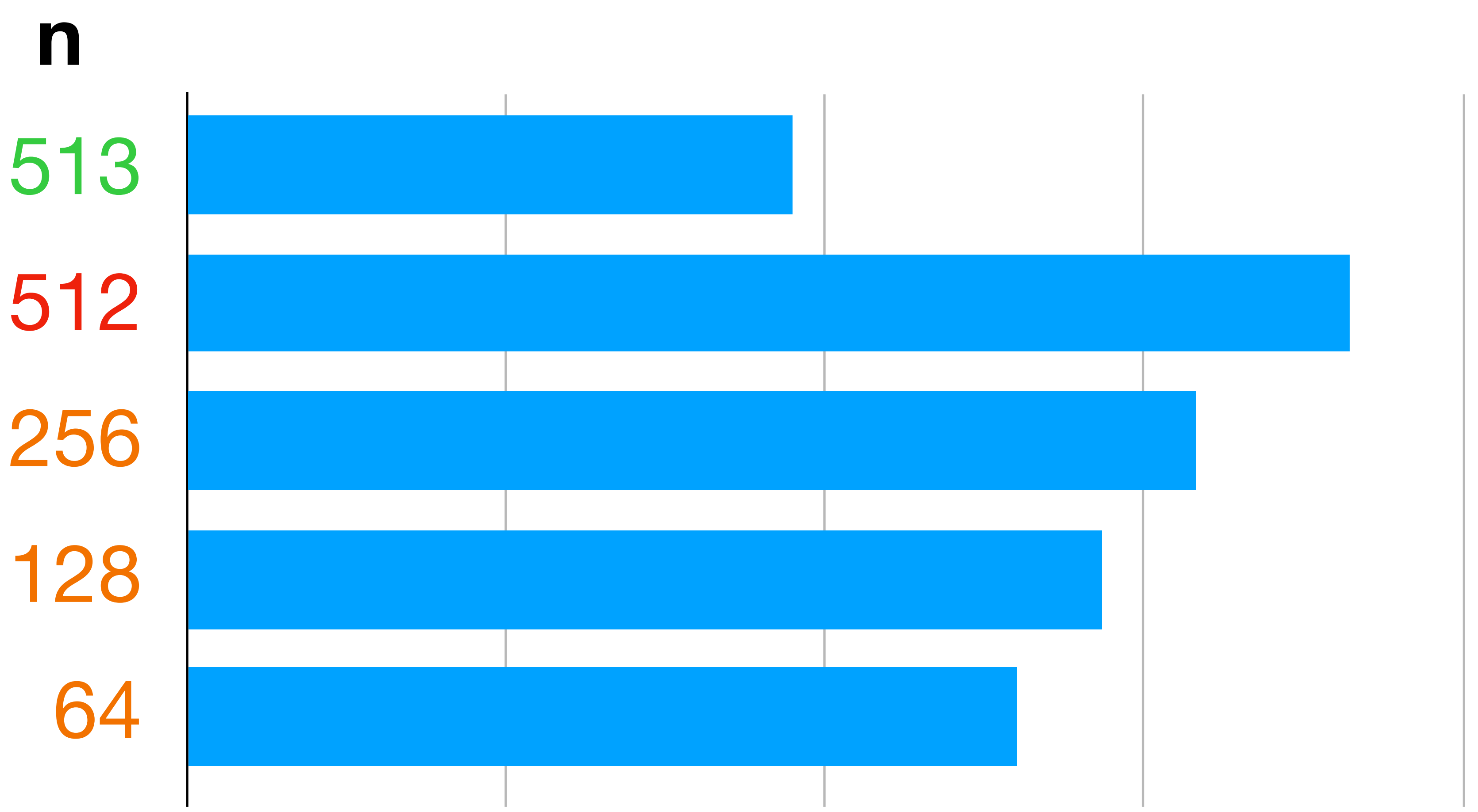

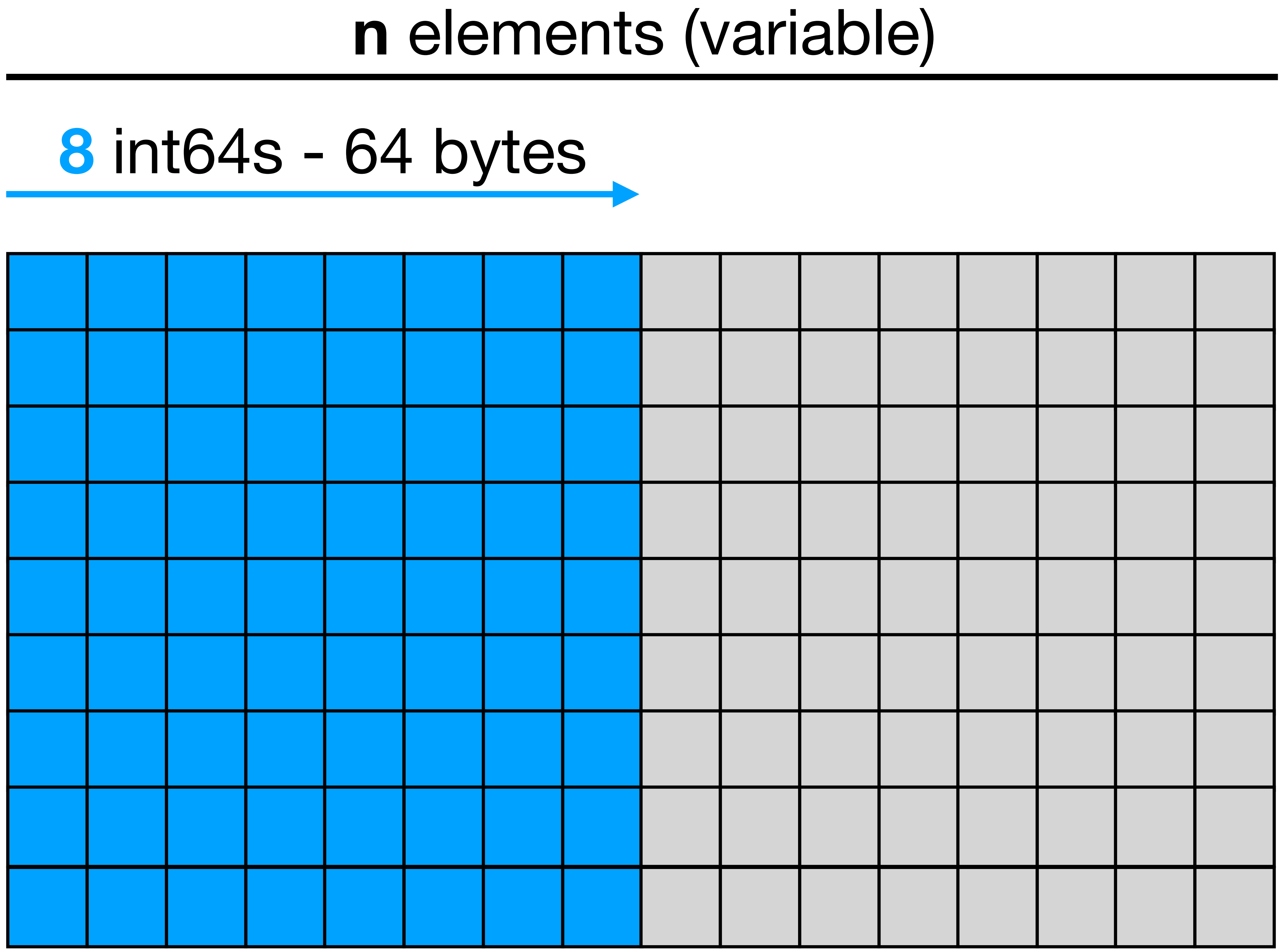

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- **Critical stride**

CPU Architecture

Locality of Reference

Data-Oriented Design

Caching Pitfall

Concurrency

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Why Concurrency?

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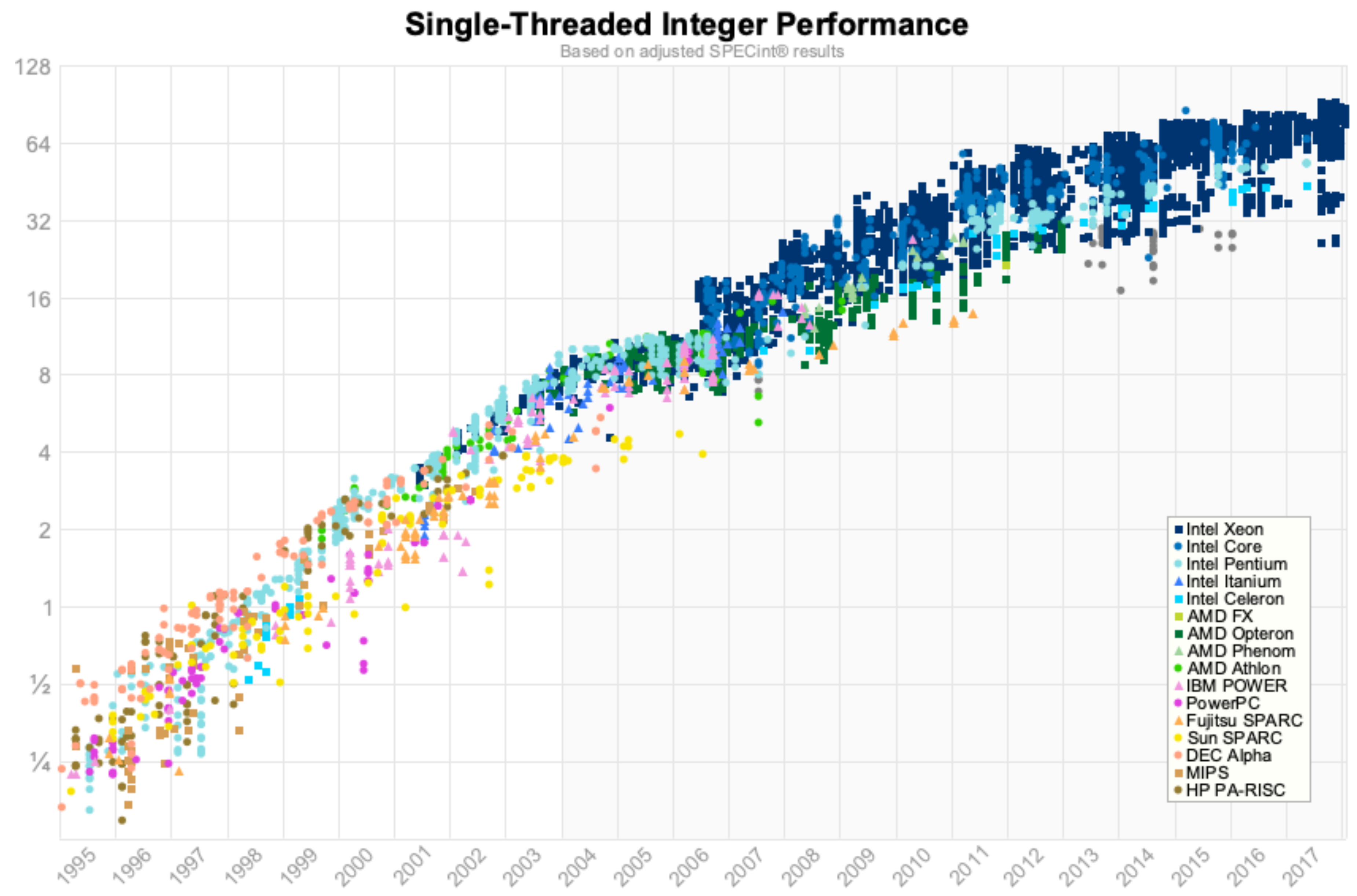

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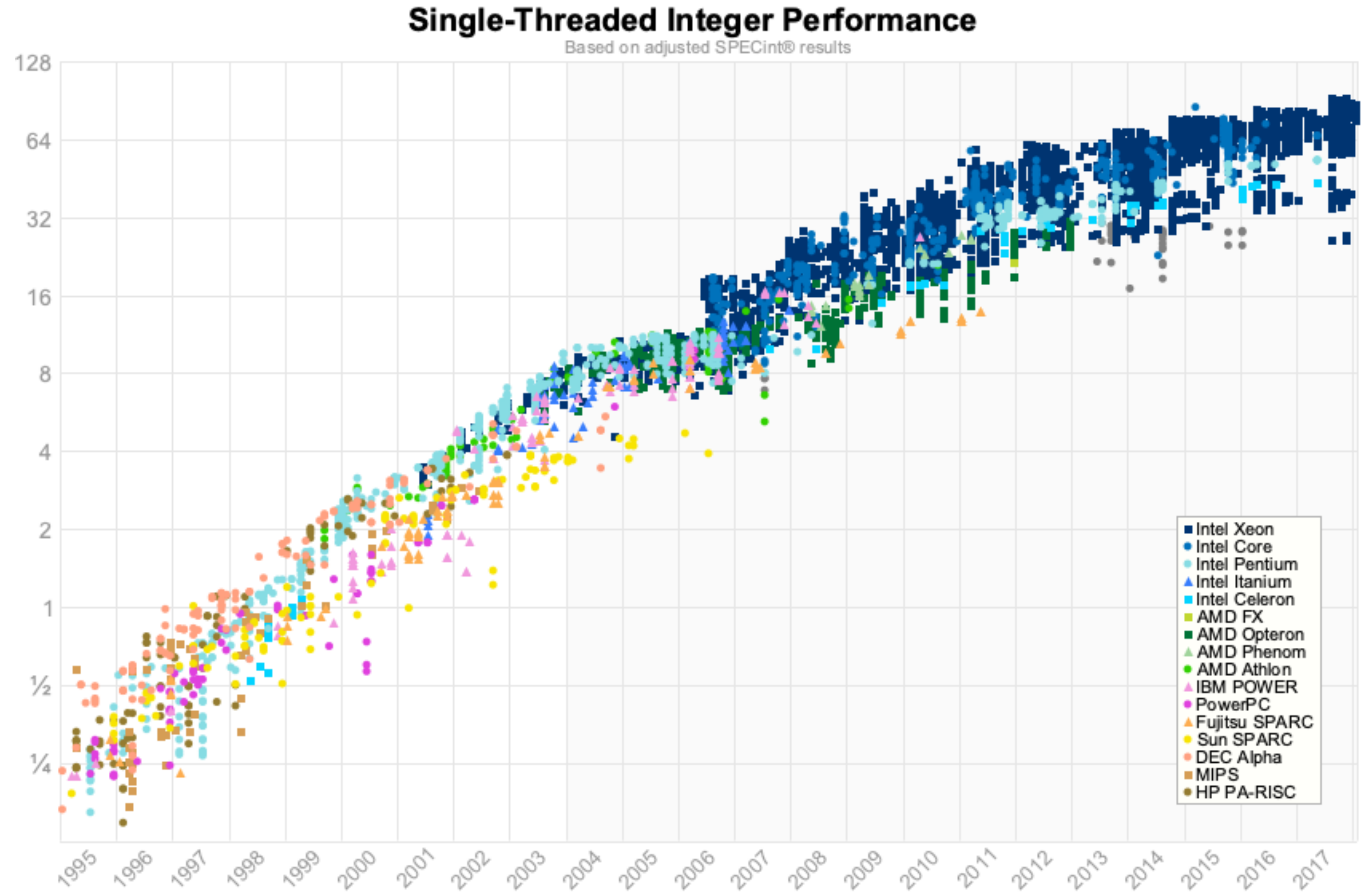

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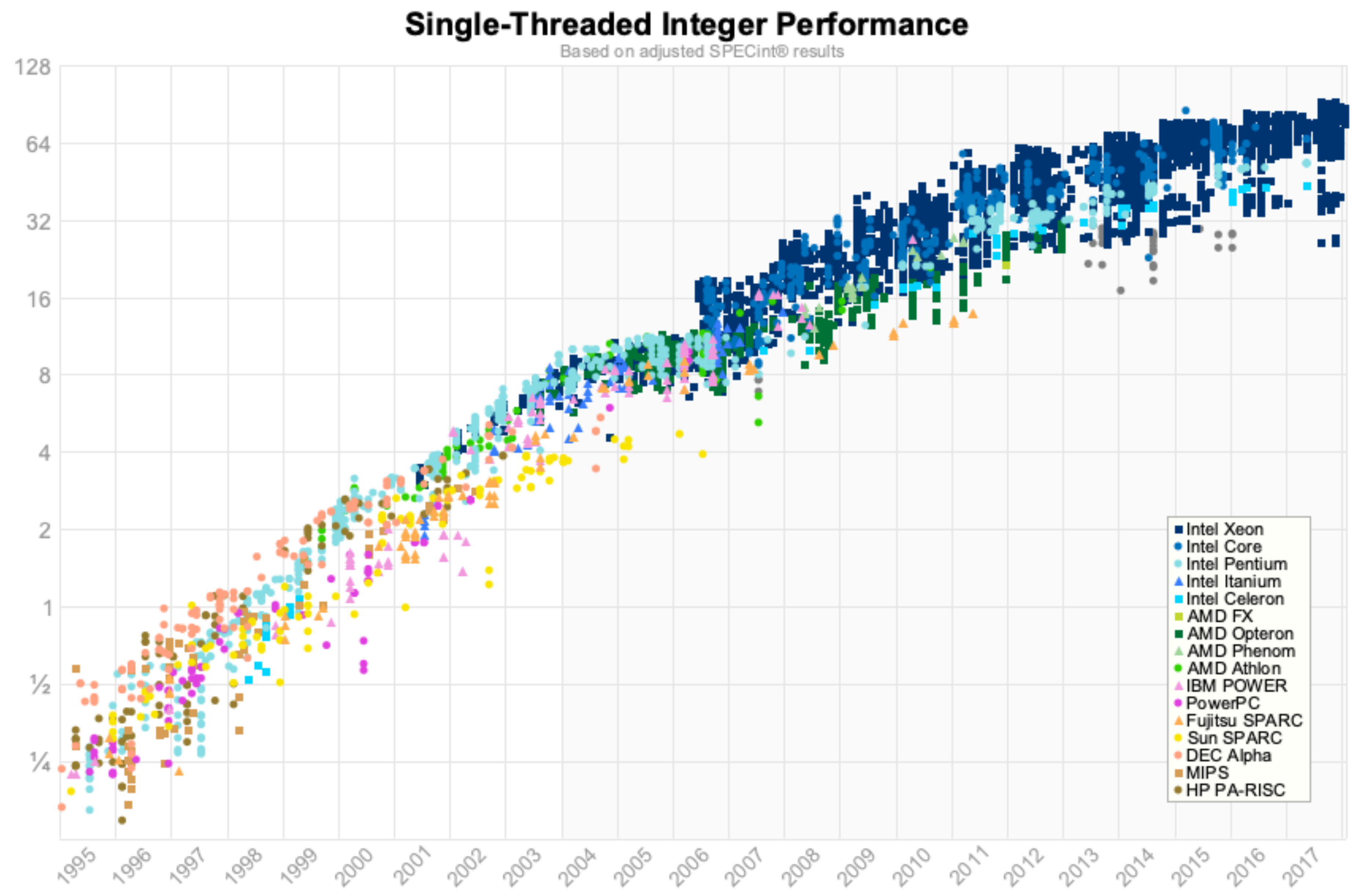

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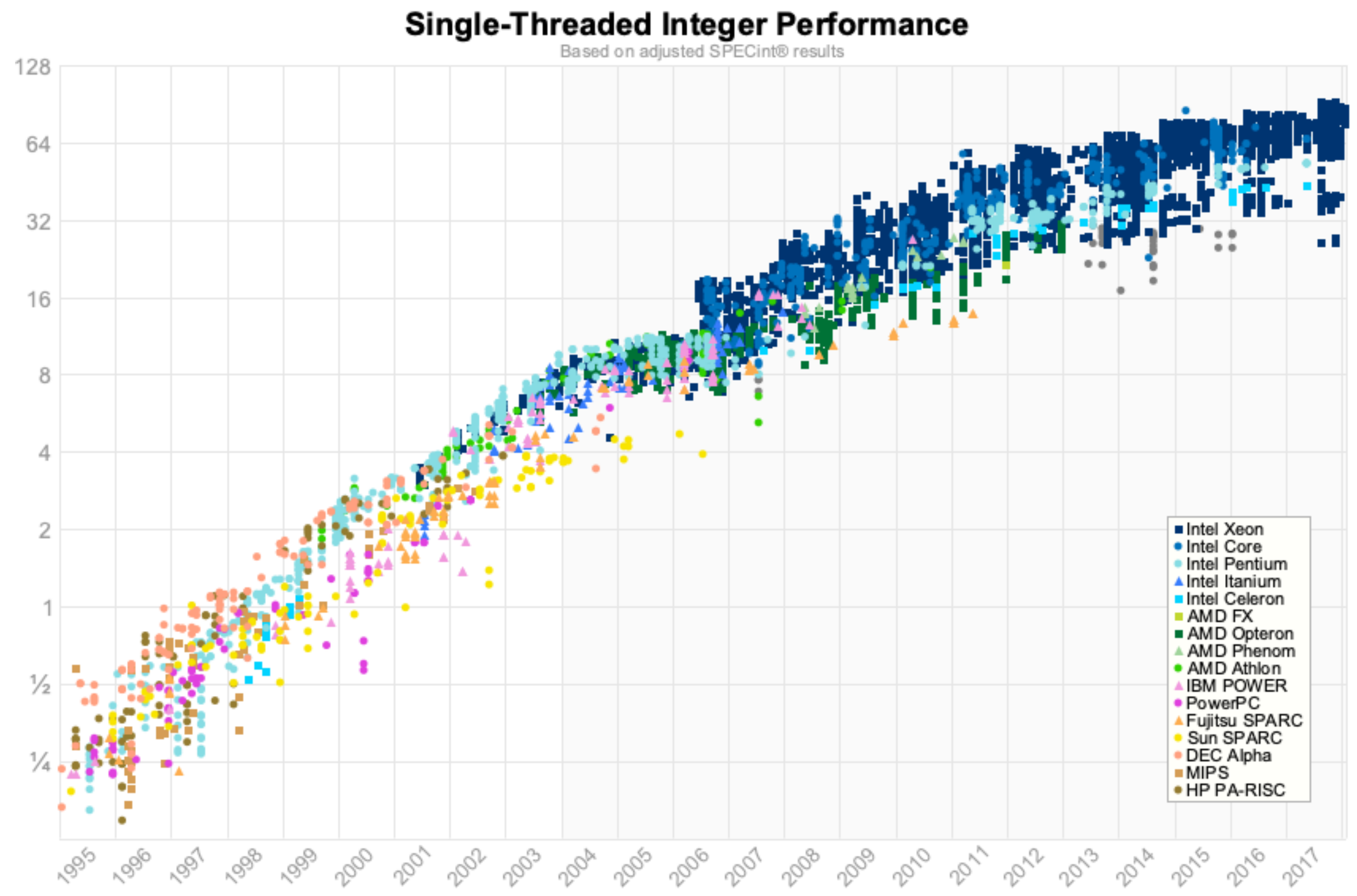

- Instead of focusing on clock speed, vendors focus on **multicores** and **hyperthreading architectures**

- <u>The free lunch is over</u> - Herb Sutter, 2005

- We cannot rely solely on the **hardware** to make our programs faster

Concurrency is the next major revolution in how we write software

```go
type Struct struct {
    n int
}

var result int

func BenchmarkIteration(b *testing.B) {
    structA := Struct{} // Initialization
    structB := Struct{} // Initialization
    wg := sync.WaitGroup{}
    b.ResetTimer()

    for i := 0; i < b.N; i++ {
        wg.Add( delta: 2)
        go func() { // Spin up first goroutine
            for j := 0; j < iteration; j++ {
                structA.n += j
            }
            wg.Done()
        }()
        go func() { // Spin up second goroutine
            for j := 0; j < iteration; j++ {
                structB.n += j
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            wg.Done()
        }()
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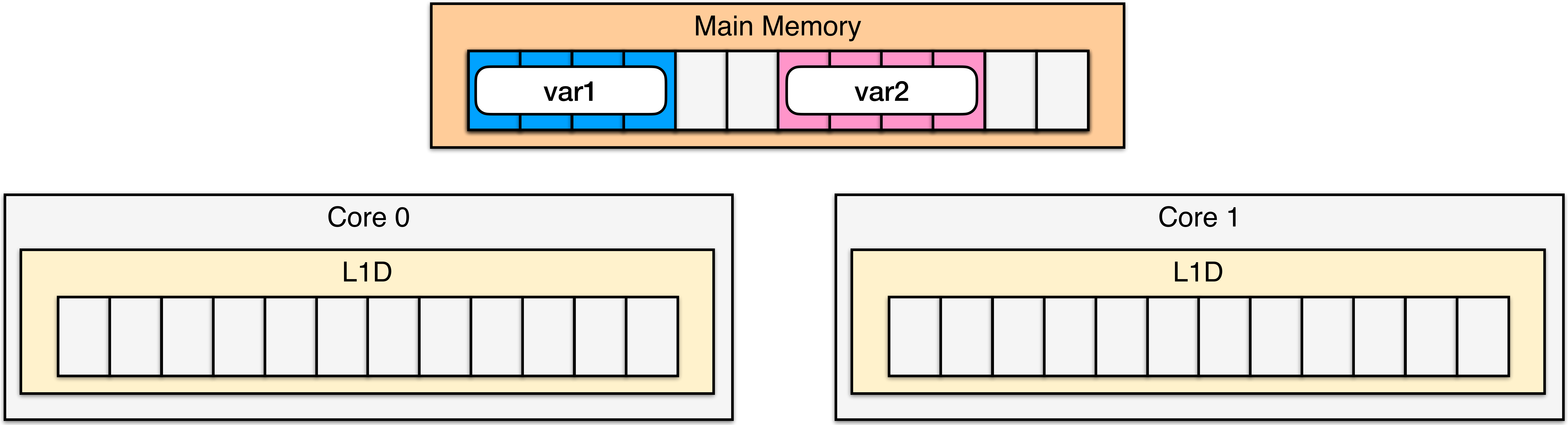
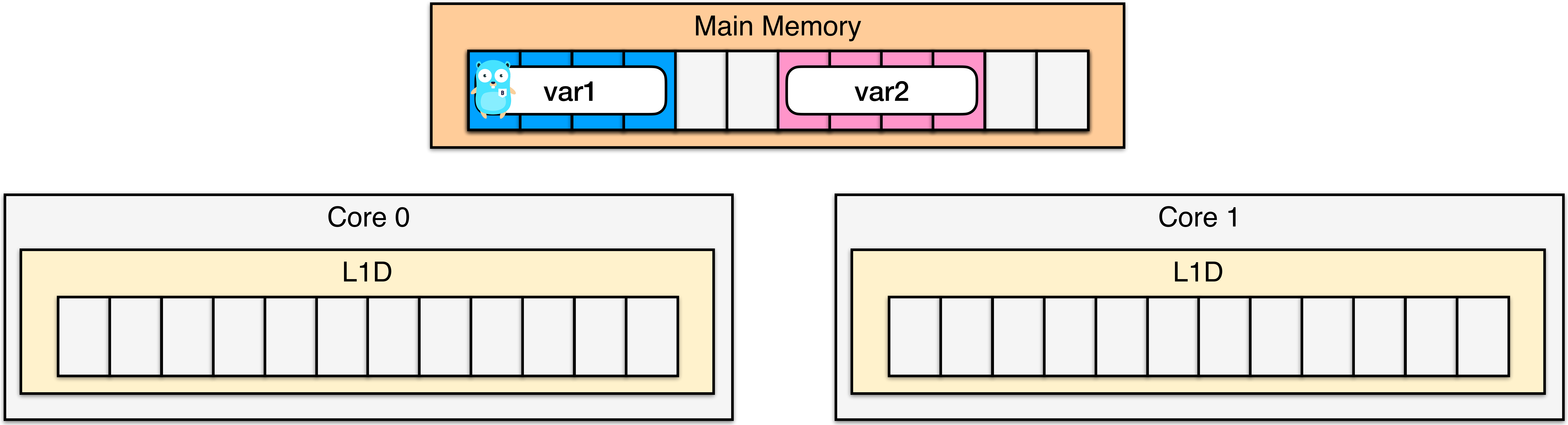
Race-free implementation!


Main Memory
var1
var2
Core 0
L1D
Core 1
L1D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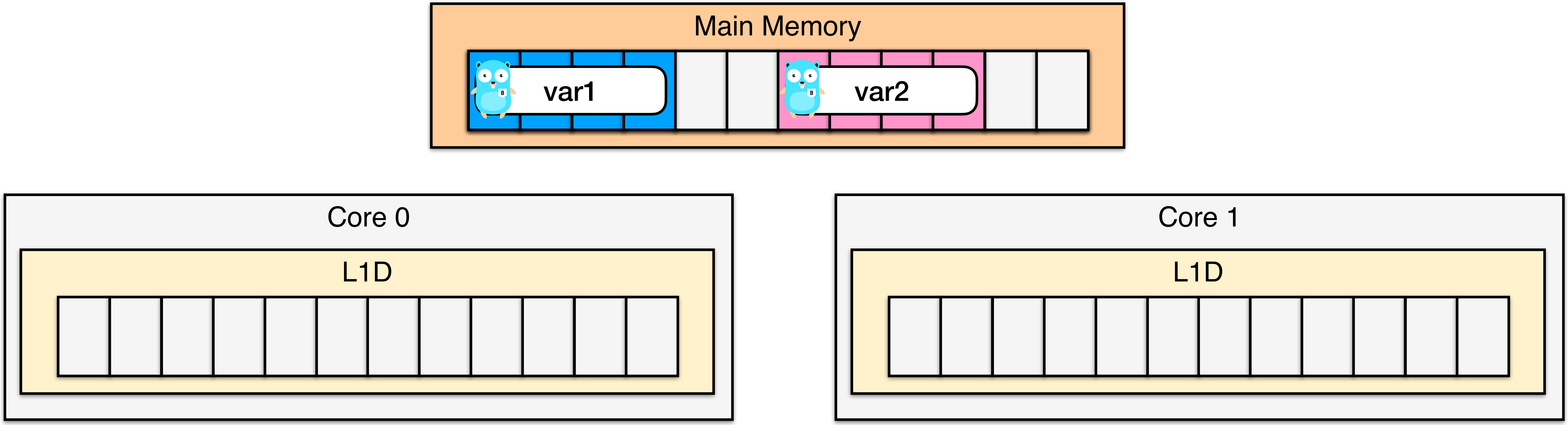

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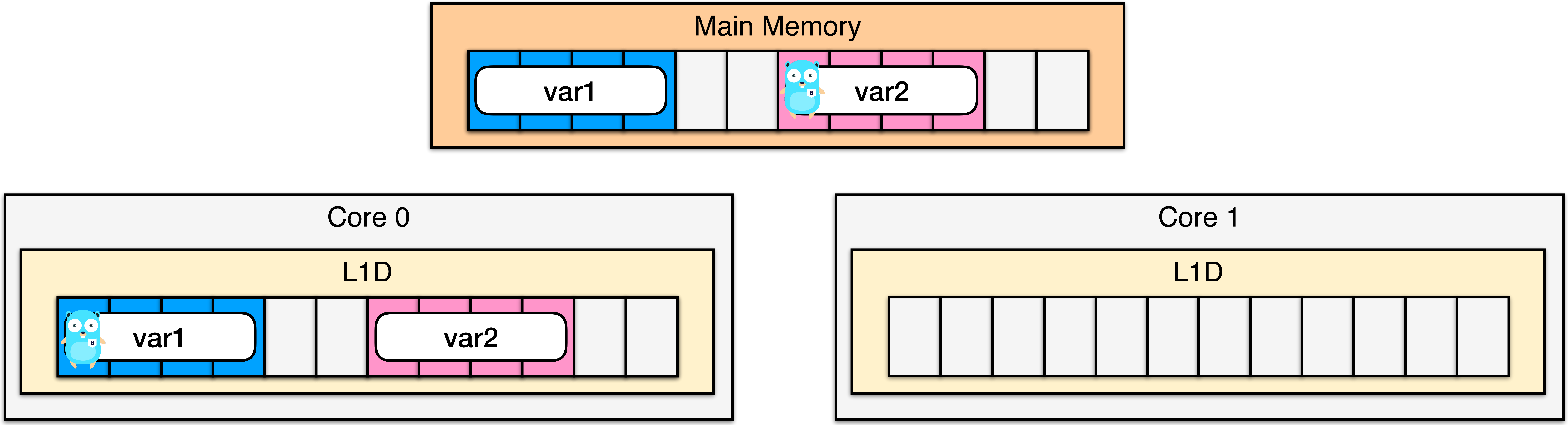

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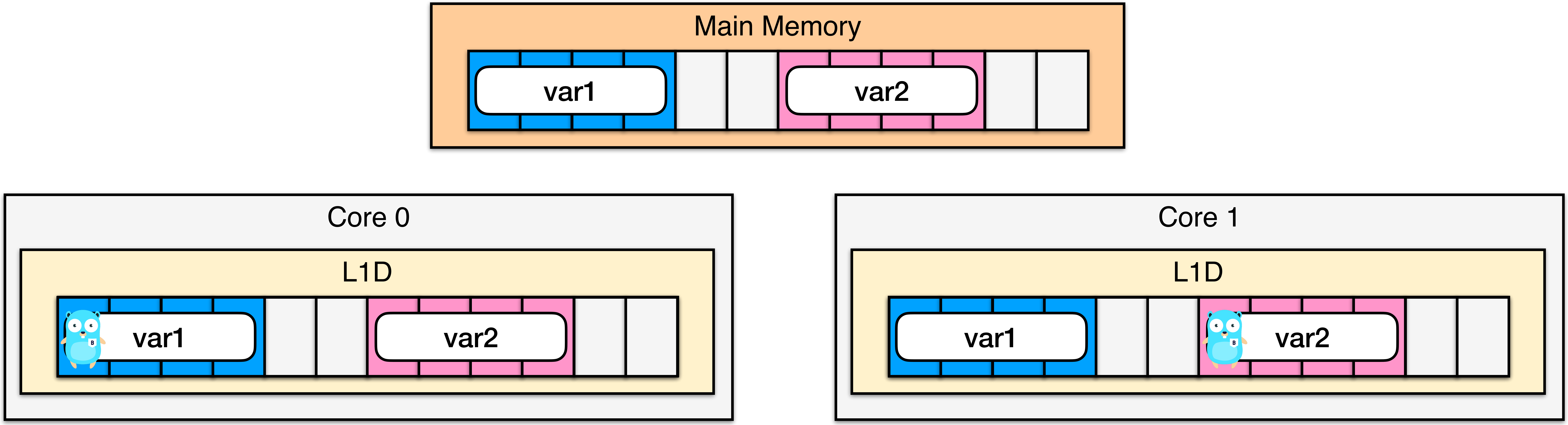
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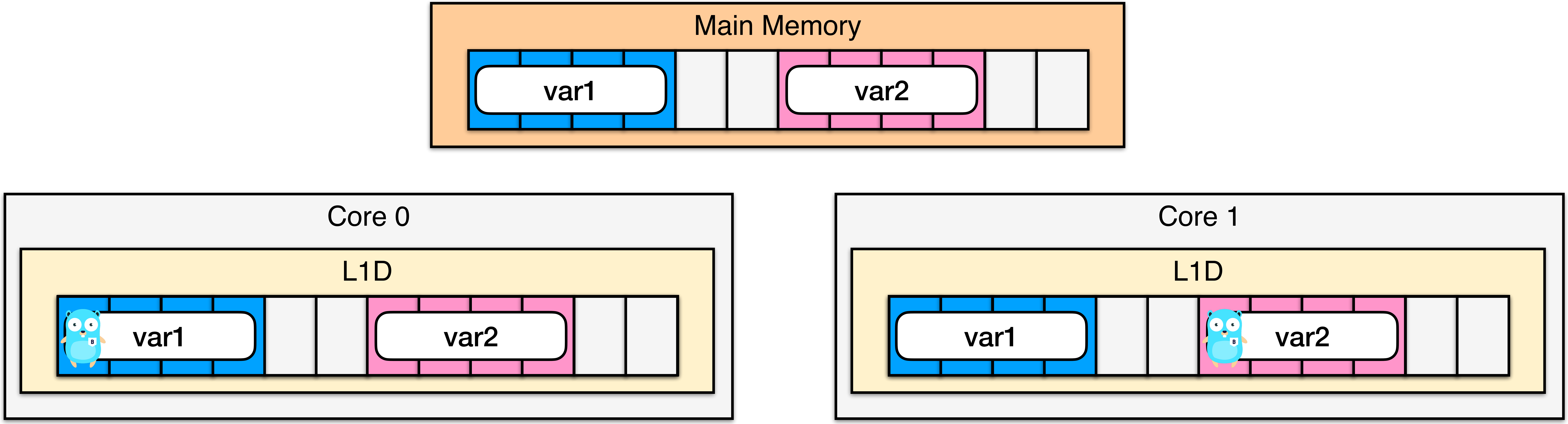
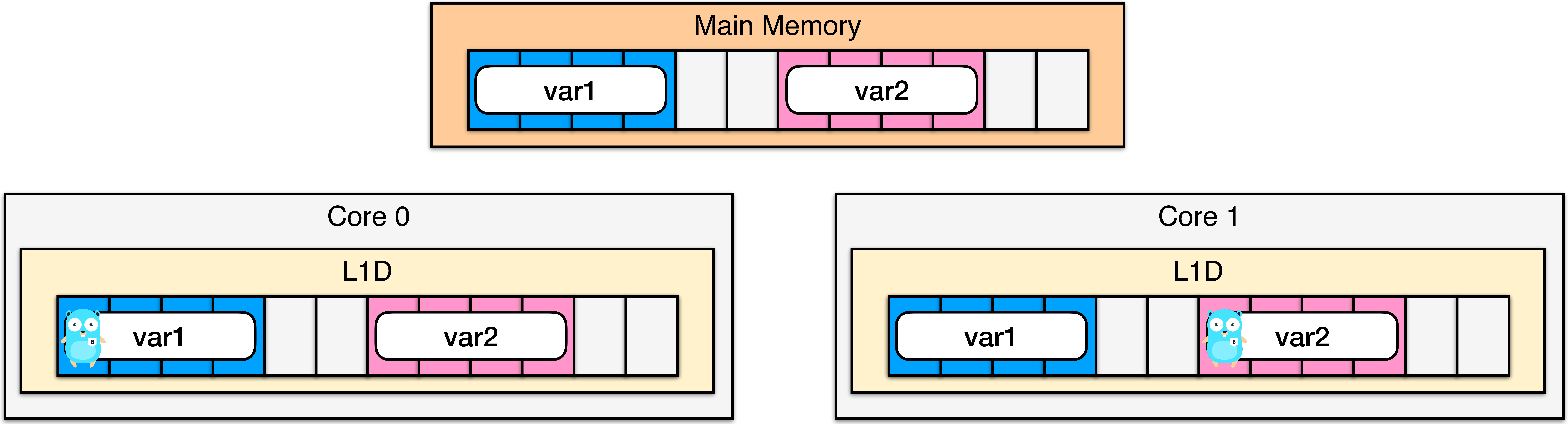
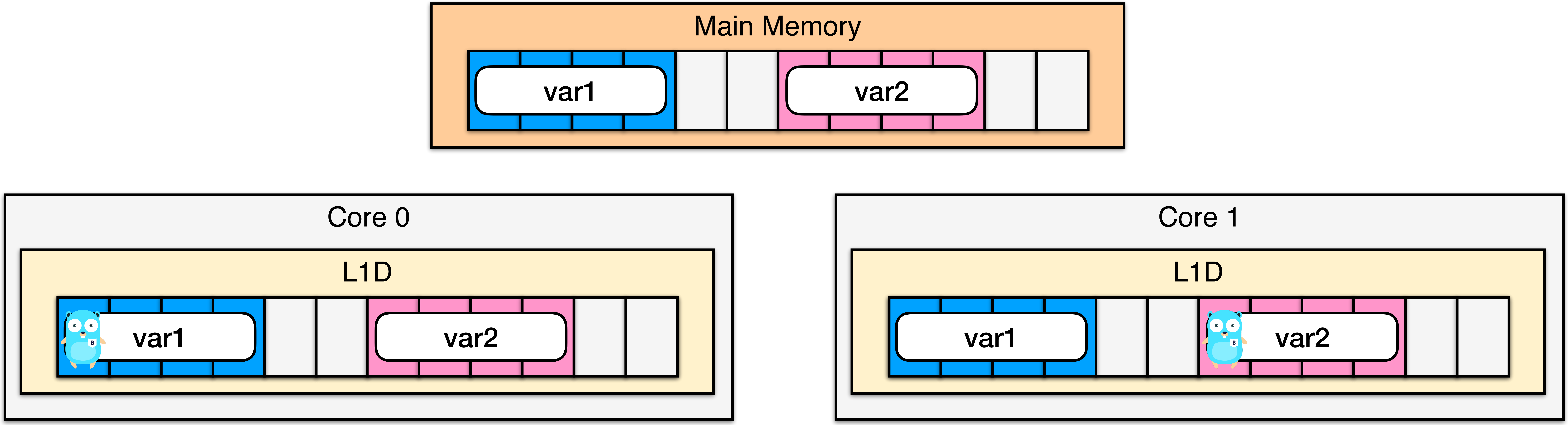


- What if both goroutines want to update their own lines



- What if both goroutines want to update their own lines
- The CPU must guarantee **cache coherency**



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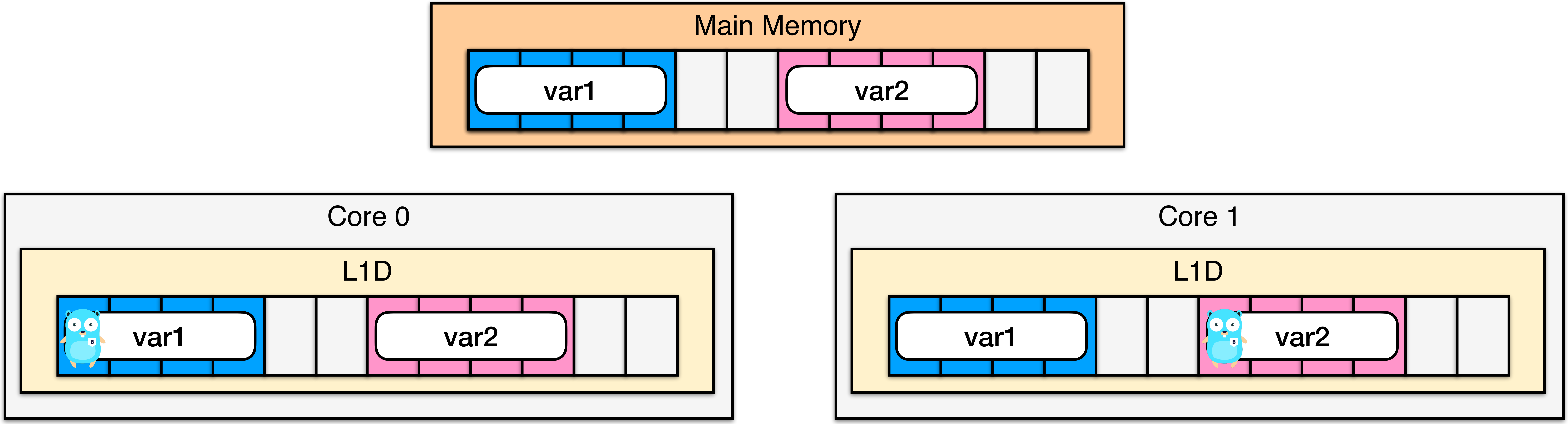
- MESI protocol (Modified, Exclusive, Shared, Invalid)



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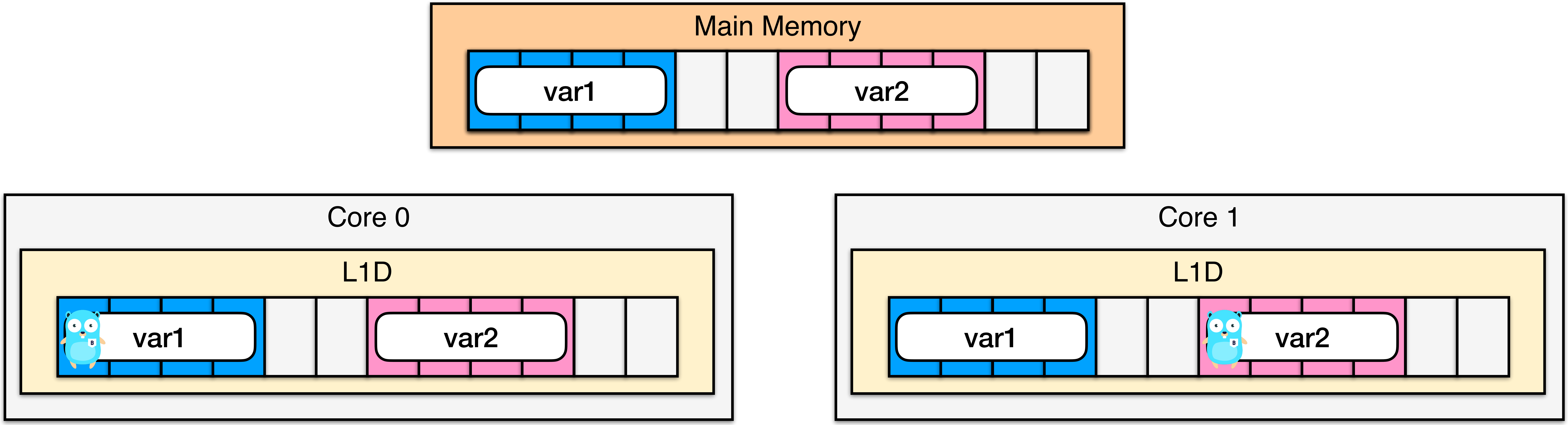

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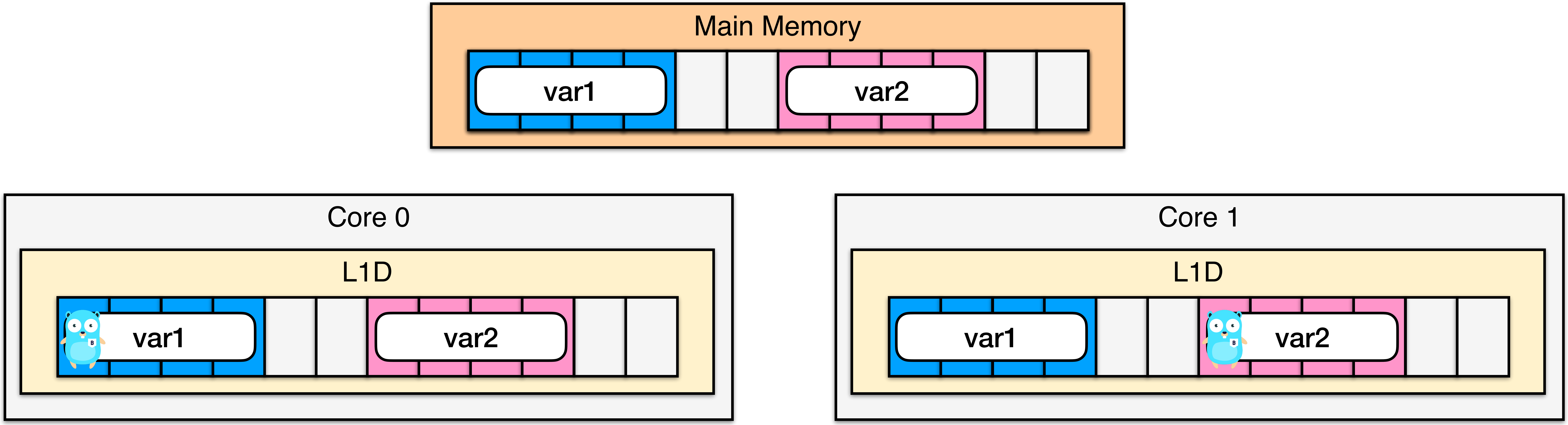

Update

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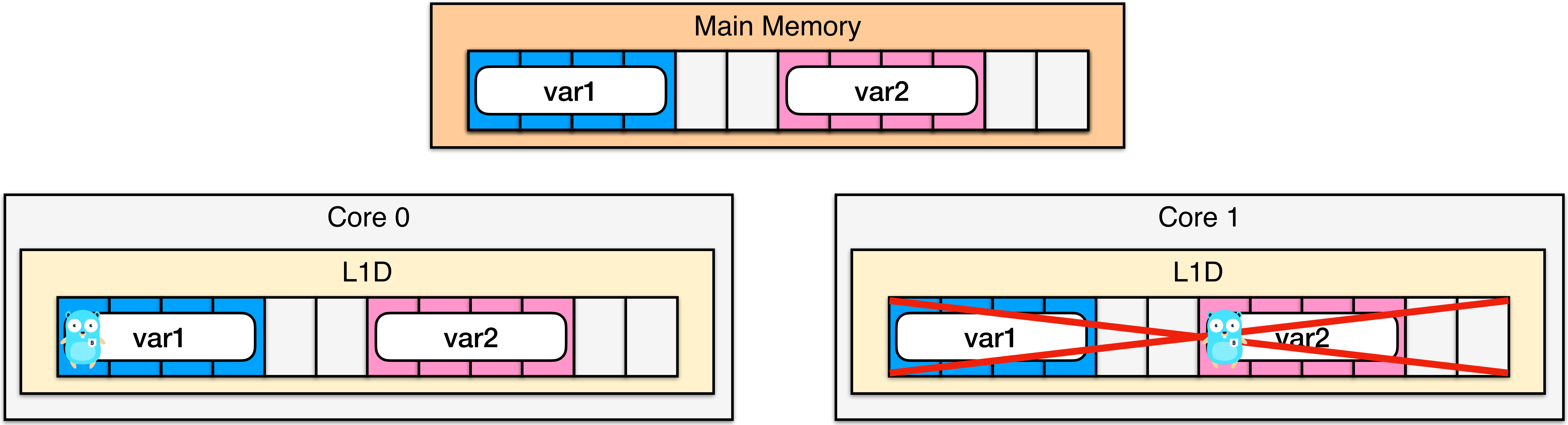

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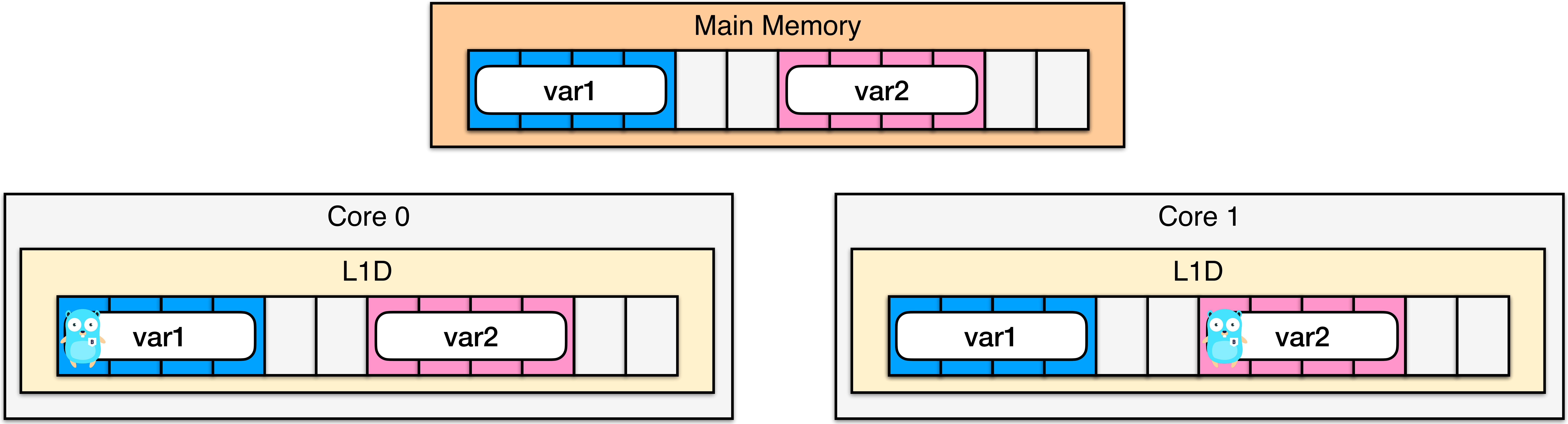

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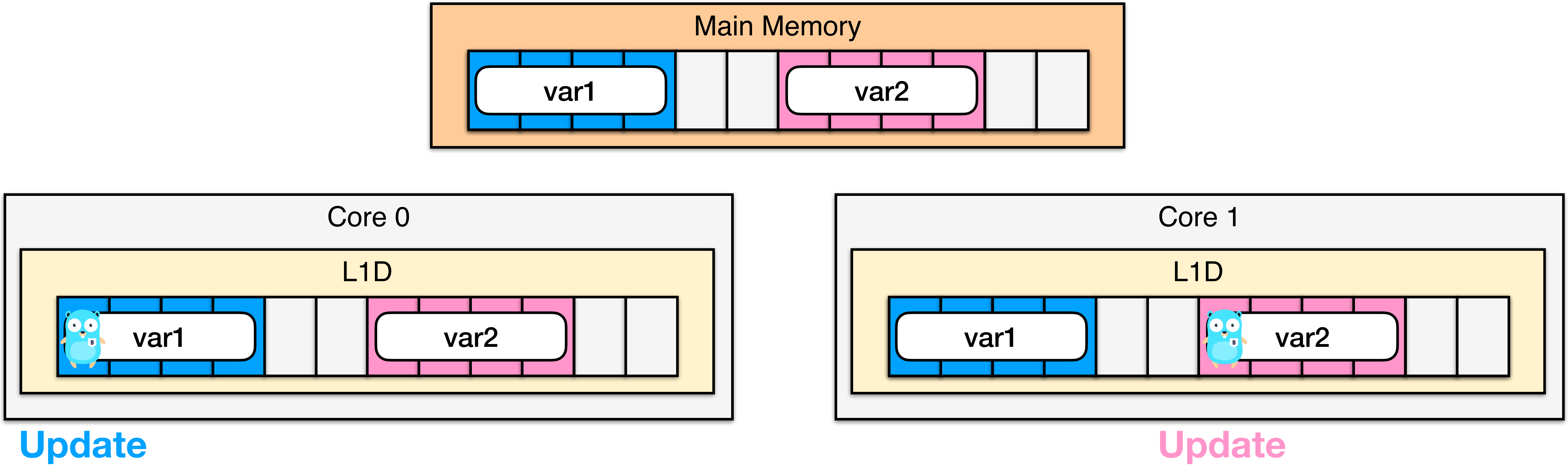

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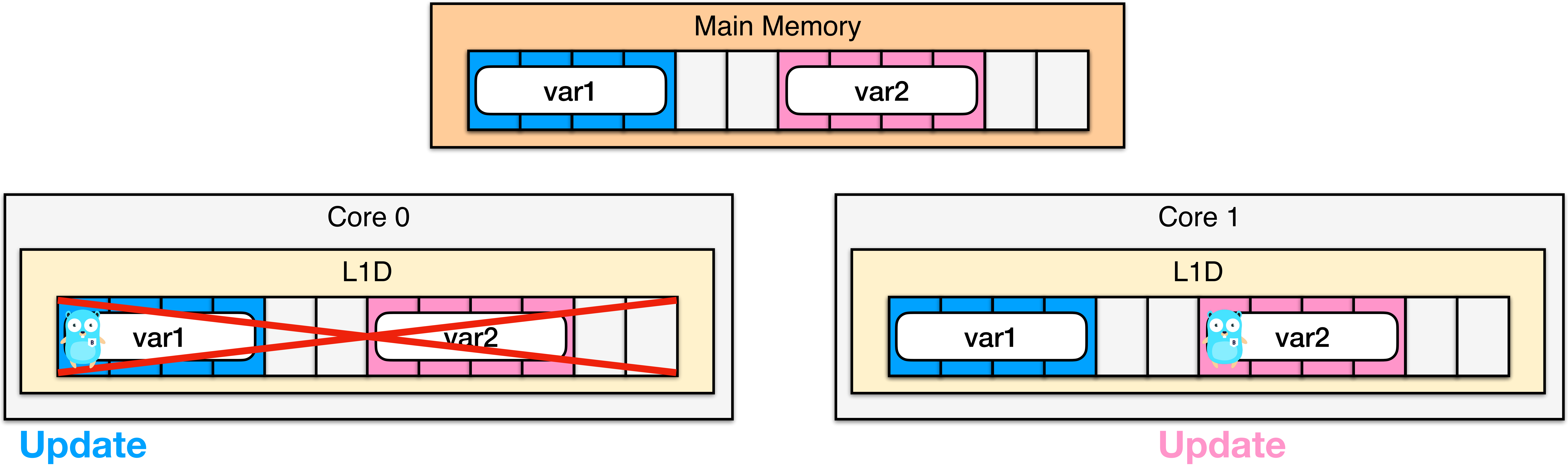

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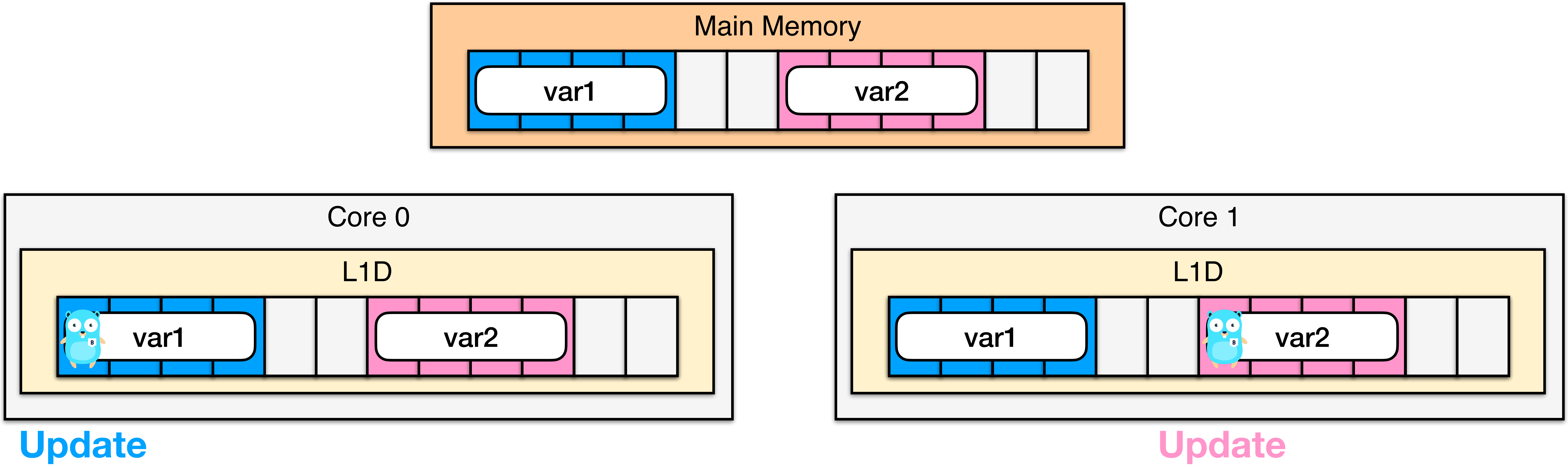

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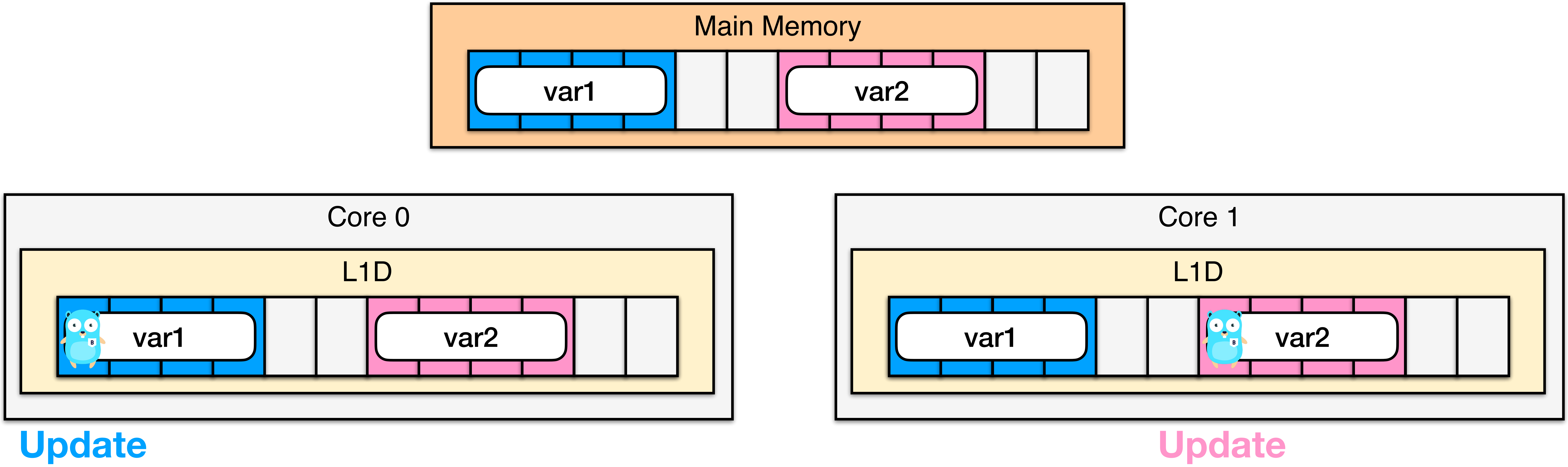
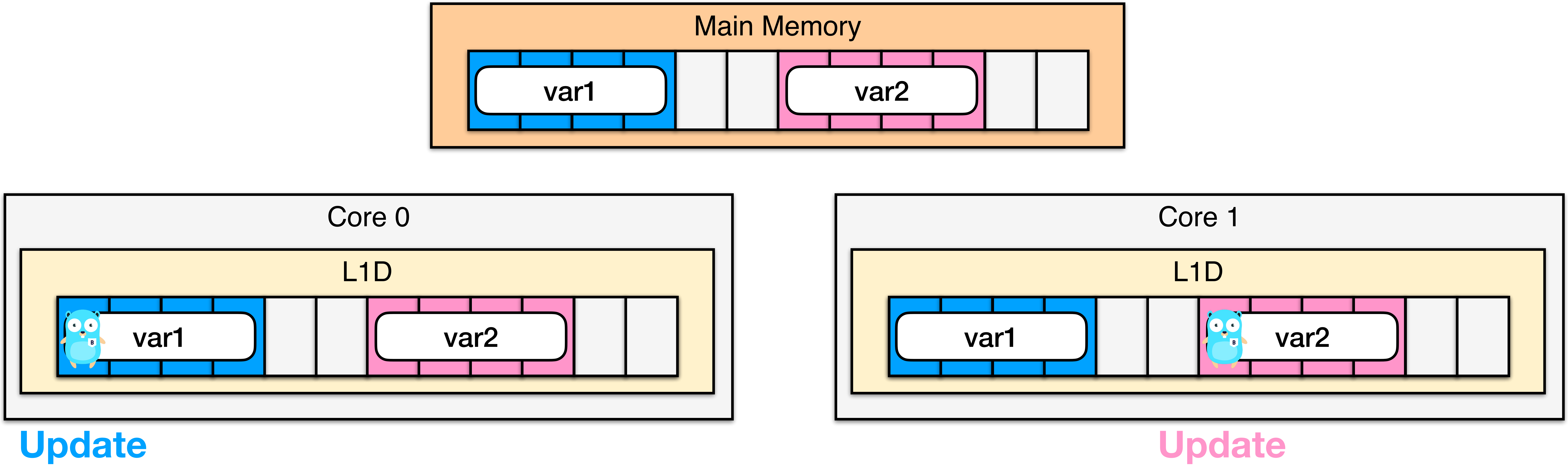


- Why does it matter?
- **False sharing** - a cache line is shared across two cores with at least one goroutine being a writer



- Why does it matter?
- **False sharing** - a cache line is shared across two cores with at least one goroutine being a writer
- Sharing memory is an **illusion**

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            wg.Done()
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structA.n and *structB.n* belongs to the **same cache line**

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- Solution 1:
  Do not communicate by sharing memory;
  instead, share memory by **communicating**

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False Sharing

- How to prevent false sharing?
- Solution 1:
  Do not communicate by sharing memory; instead, share memory by **communicating**


```go
func BenchmarkIterationCommunication(b *testing.B) {
    ch := make(chan int, 2)
    for i := 0; i < b.N; i++ {
        go func() { // Spin up first goroutine
            i := 0 // Local state
            for j := 0; j < iteration; j++ {
                i += j
            }
            ch <- i
        }()
        go func() { // Spin up second goroutine
            i := 0 // Local state
            for j := 0; j < iteration; j++ {
                i += j
            }
            ch <- i
        }()
        result = <-ch + <-ch // Wait and aggregate
    }
}
```

False Sharing

- How to prevent false sharing?

- Solution 1:
  Do not communicate by sharing memory; instead, share memory by **communicating**


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func BenchmarkIterationCommunication(b *testing.B) {
    ch := make(chan int, 2)
    for i := 0; i < b.N; i++ {
        go func() { // Spin up first goroutine
            i := 0 // Local state
            for j := 0; j < iteration; j++ {
                i += j
            }
            ch <- i
        }()
        go func() { // Spin up second goroutine
            i := 0 // Local state
            for j := 0; j < iteration; j++ {
                i += j
            }
            ch <- i
        }()
        result = <-ch + <-ch // Wait and aggregate
    }
}
```

False Sharing

- How to prevent false sharing?

- Solution 1:
  Do not communicate by sharing memory;
  instead, share memory by **communicating**


```go
func BenchmarkIterationCommunication(b *testing.B) {
    ch := make(chan int, 2)
    for i := 0; i < b.N; i++ {
        go func() { // Spin up first goroutine
            i := 0 // Local state
            for j := 0; j < iteration; j++ {
                i += j
            }
            ch <- i
        }()
        go func() { // Spin up second goroutine
            i := 0 // Local state
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False Sharing

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```go
type PaddedStruct struct {
    _ cpu.CacheLinePad
    n int
    _ cpu.CacheLinePad
}

func BenchmarkIterationWithPadding(b *testing.B) {
    structA := PaddedStruct{} // Initialization
    structB := PaddedStruct{} // Initialization
    wg := sync.WaitGroup{}
    b.ResetTimer()

    for i := 0; i < b.N; i++ {
        wg.Add( delta: 2)
        go func() { // Spin up first goroutine
            for j := 0; j < iteration; j++ {
                structA.n += j
            }
            wg.Done()
        }()
        go func() { // Spin up second goroutine
            for j := 0; j < iteration; j++ {
                structB.n += j
            }
            wg.Done()
        }()
        wg.Wait() // Wait
    }
}
```

False Sharing

- How to prevent false sharing?
- Solution 2: **padding**

```go
type PaddedStruct struct {
    _ cpu.CacheLinePad // 64 bytes
    n int
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            }
            wg.Done()
        }()
        go func() { // Spin up second goroutine
            for j := 0; j < iteration; j++ {
                structB.n += j
            }
            wg.Done()
        }()
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    }
}
```

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False Sharing

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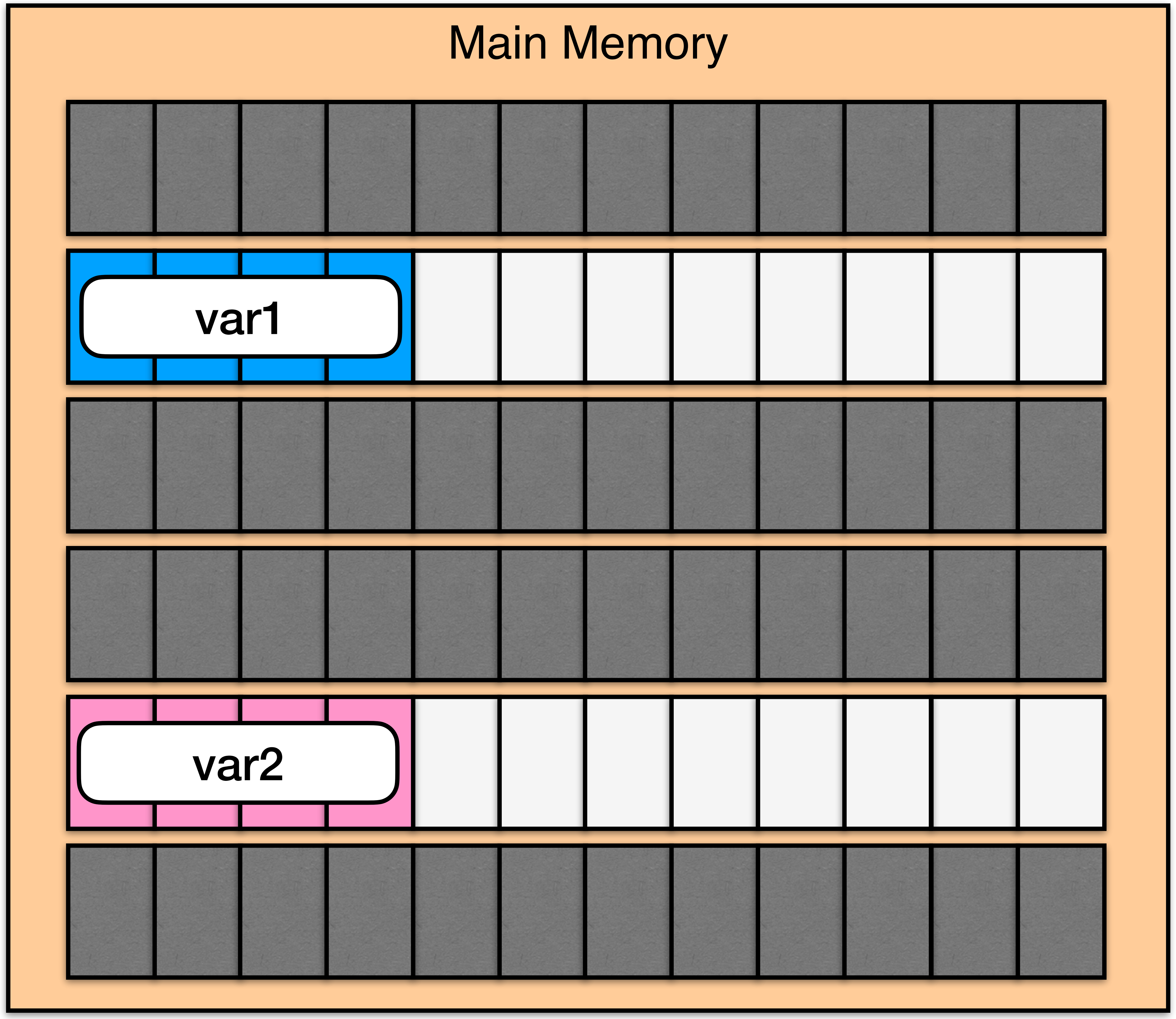
- Solution 2: **padding**

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False Sharing

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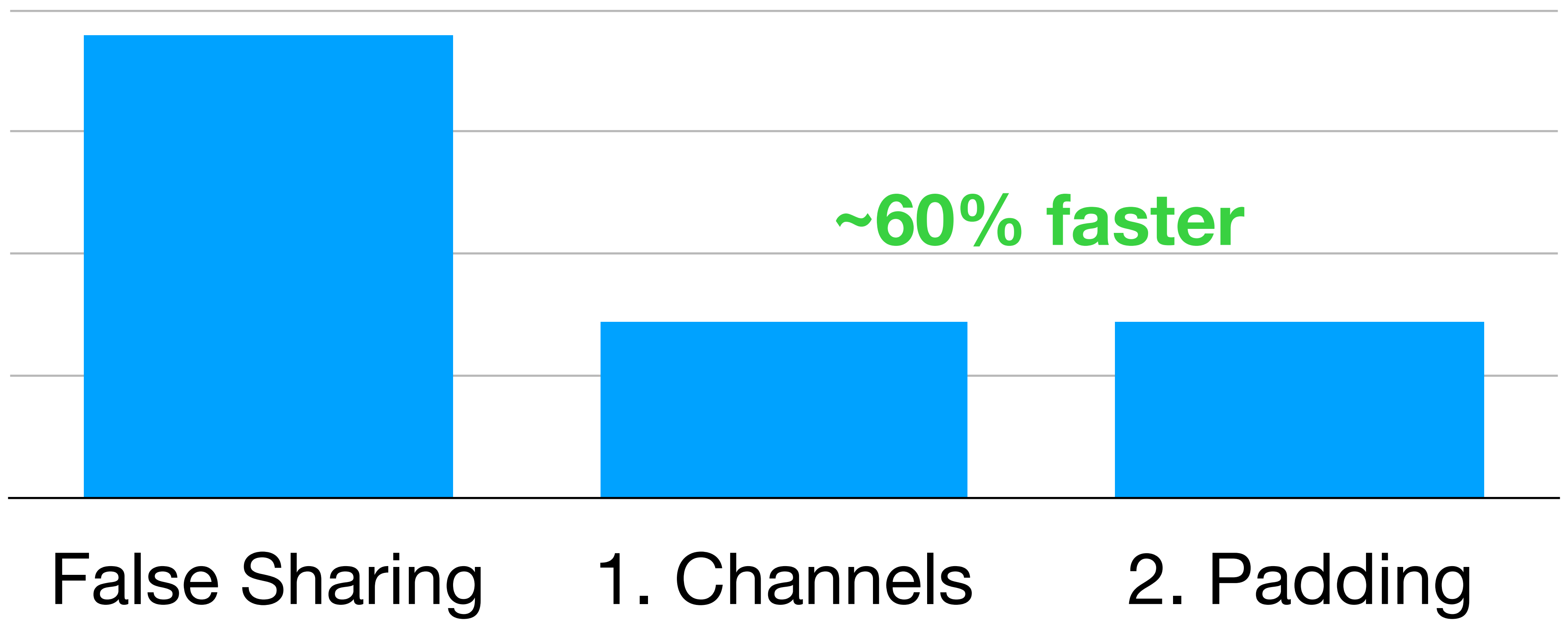

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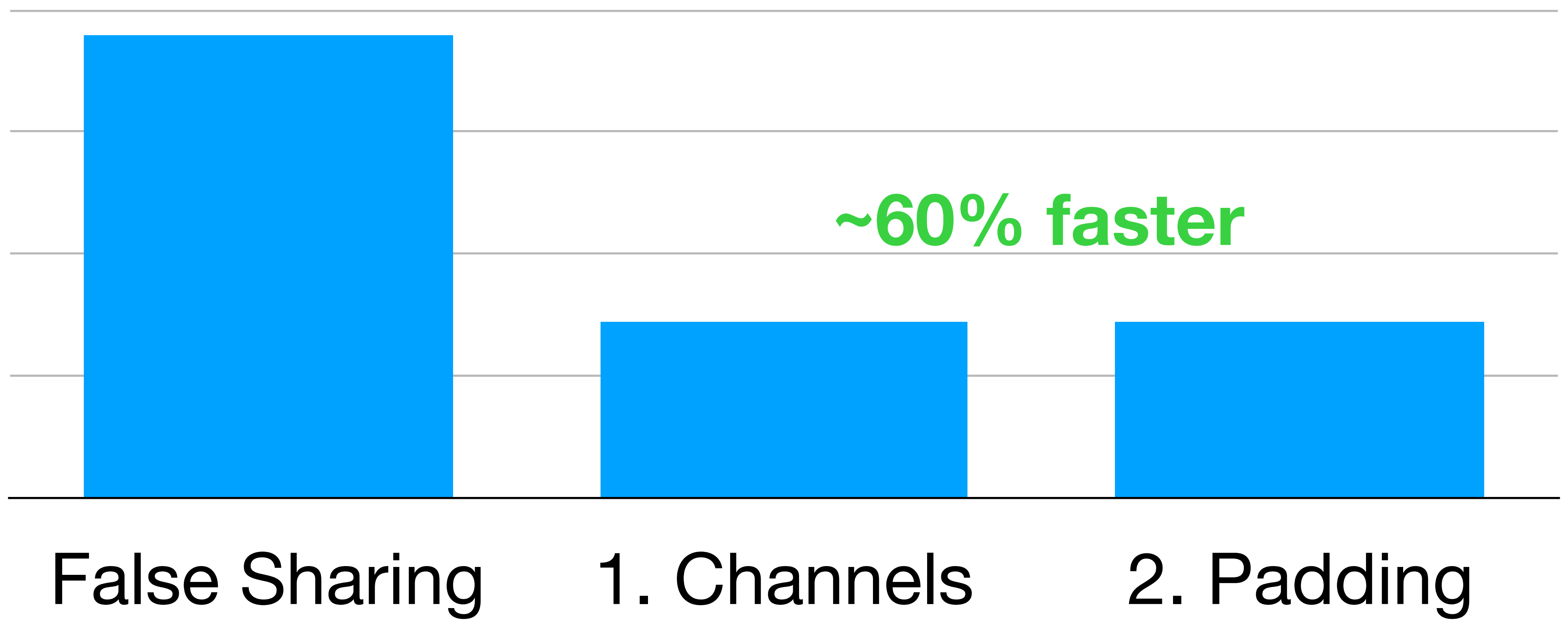

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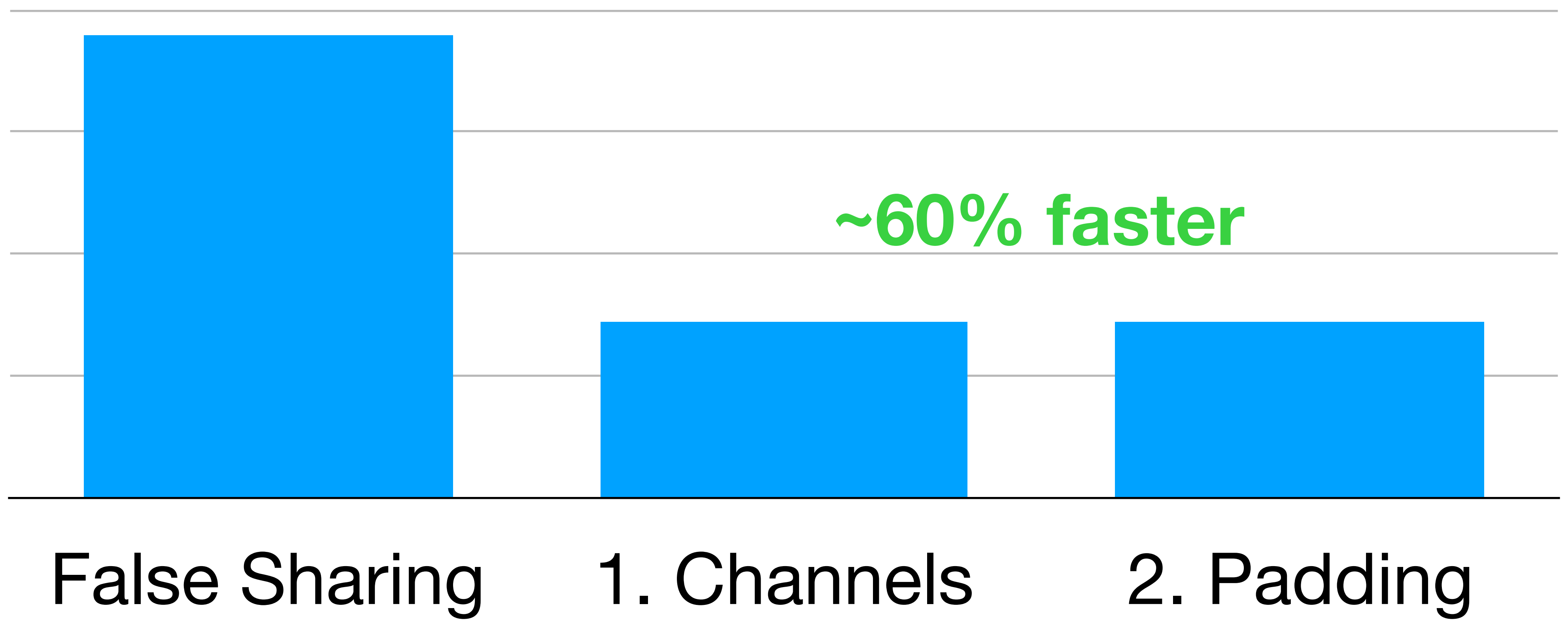

- <u>Padding is hard</u> - Dave Cheney
- Sometimes, padding is **necessary**. E.g. we are obliged to share memory and we want to prevent false sharing (library, etc.).

Conclusion

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  - False sharing
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What else?

- Watch out for premature:
  - Optimisations

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- A code that looks perfectly valid might still be **problematic** at CPU level:
  - Caching distribution
  - False sharing
- We can help the CPU with **locality of reference** and **predictability** (algorithms & data structures)

What else?

- Watch out for premature:
  - Optimisations
  - Concurrency
- Mechanical sympathy goes beyond the very scope of CPUs

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Thank You

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